AS1181

Datasheet

Published by ams-OSRAM AG
Tobelbader Strasse 30, 8141 Premstaetten, Austria
Phone +43 3136 500-0
ams-osram.com

OSRAM

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AS1181 8-channel LED/VCSEL driver with enhanced safety features

1 General description

AS1181 is an 8-channel highly integrated self-contained LED/VCSEL driver for near to eye applications such as Augmented Reality (AR) and Virtual Reality (VR) glasses. The device integrates extended safety monitoring functions to ensure eye safe operation. These safety monitors include LED short detection, LED open detection, LED overcurrent protection, LED on time monitor as well as temperature shutdown and a built-in-self test (BIST).

The device is configurable via a serial wire interface (I^2C or I3C) with interrupt and provides two Strobe/PWM inputs to synchronize illumination with up to two external cameras for binocular eye tracking systems.

The LED current is individually programmable per channel, and it can drive up to 2 IR LEDs per current sink with a minimum ON time of 10µs and a maximum current of 66mA per channel.

General purpose LED driving applications can be supported via a direct PWM input applied at the Strobe pin and it can drive RGB or white LEDs considering a maximum forward voltage of 5V.

The device comes in a tiny wafer-level-chip-scale package (WLCSP) with 0.4mm pitch and dimensions of 2.9mm x 1 .75mm x 0.5mm (L x W x H).

1.1 Key benefits & features

The benefits and features of AS1181, 8-channel LED/VCSEL driver with enhanced safety features are listed below:

Table 1: Added value of using AS1181

Benefits	Features
Fully self-contained fault detection and protection enables easier implementation of eye safety functionality in end devices over discrete solutions.	Enhanced safety monitors: • High side over current detection (Anode) • High side LP node short detection (Anode) • Low side open/short LED detection (Cathode) • Built-in-self test (BIST) • Illumination time monitor • Over & low temperature shutdown
Easy integration into size constraint applications	Tiny WL-CSP 28 package with 0.4mm pitch. 2.9mm x 1.75mm x 0.5mm (L x W x H)
Support for binocular eye tracking systems	Dual trigger input to start and synchronize illumination with two eye tracking cameras.

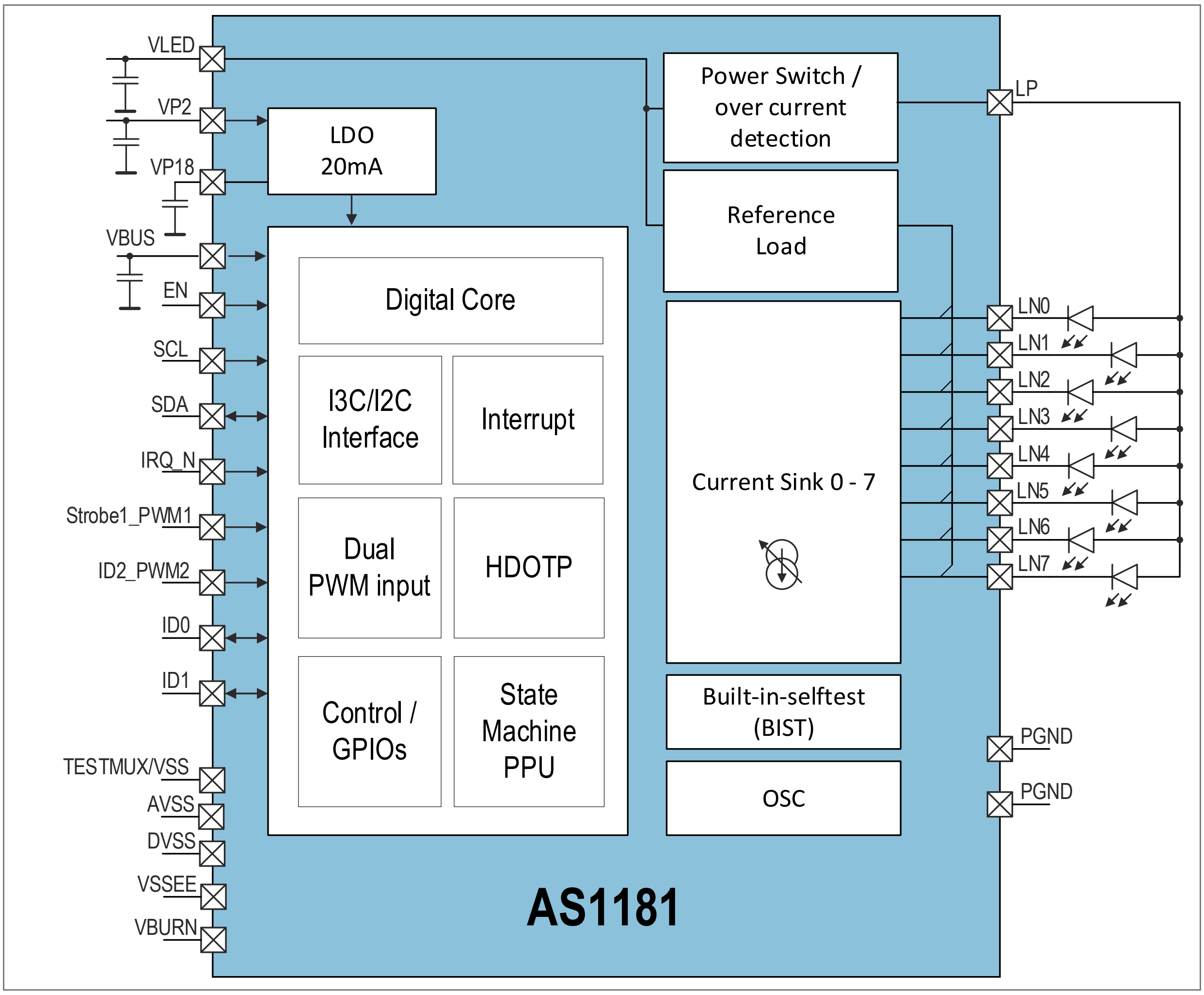
1.2 Applications

- Eye- / face / hand tracking in AR/VR and XR glasses
- Iris recognition
- General purpose LED driver with enhanced safety features

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of AS1181



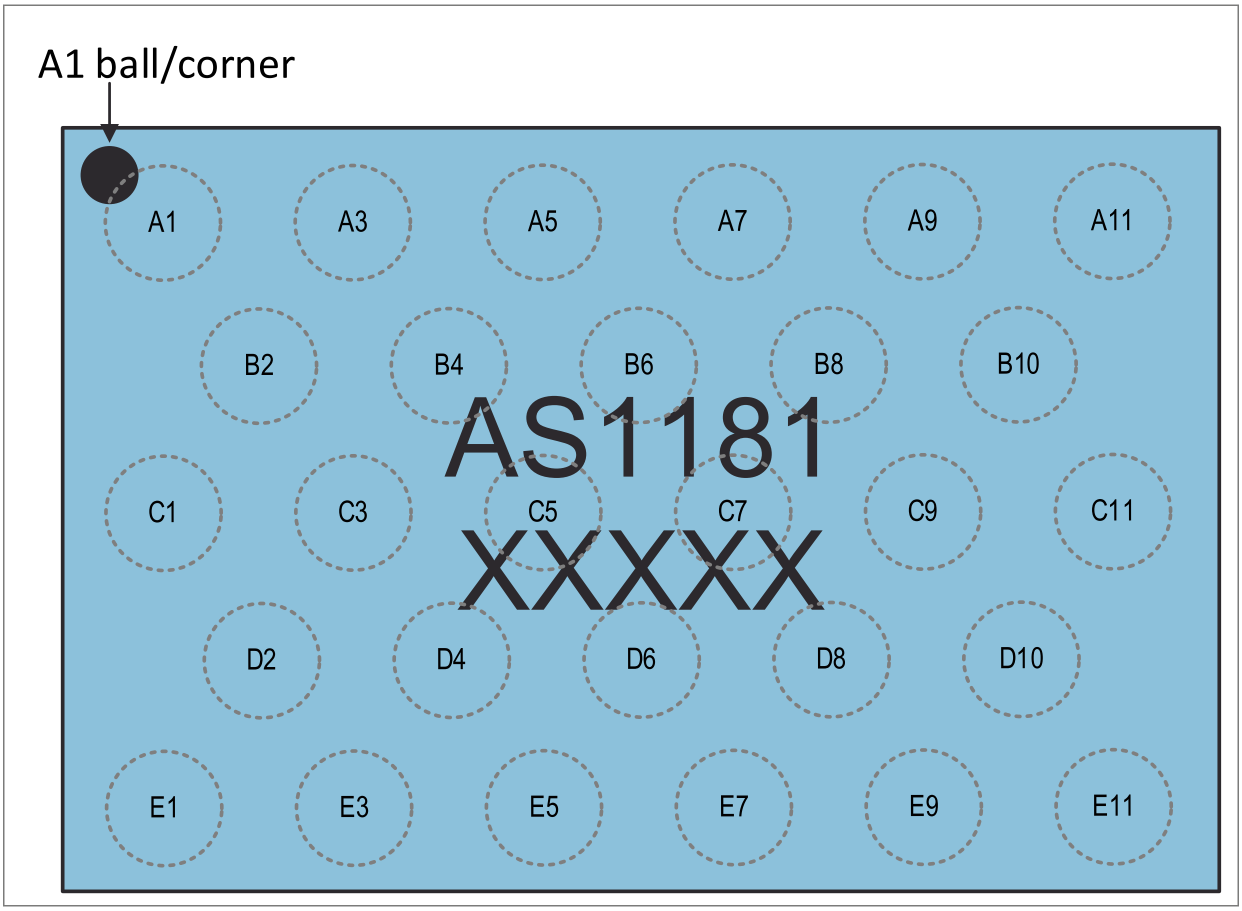
2 Ordering information

Ordering code	Package	Product type/Marking	Delivery form	Delivery quantity
Q65113A9356	WLCSP-28	AS1181	Tape & reel	1000 pcs/reel
Q65115A2377	WLCSP-28	AS1181	Tape & reel	4000 pcs/reel

3 Pin assignment

3.1 Pin diagram

Figure 2: Pin diagram of AS1181



3.2 Pin description

Table 2: Pin description of AS1181

Pin number	Pin name	Pin type[(1)]	Description
A1	LP	AIO	Anode LED connection (High Side Current Monitor Output)
A3	VSS_EE	PWR	Connect to ground
A5	SCL	DI	I²C /I3C clock
A7	ID2_PWM2	DI	ID2 pin or / PWM2 input
A9	IRQ_N	DO	Interrupt output
A11	STROBE1_PWM1	DI	STROBE input or / PWM1 input
B2	VBURN	PWR	HDOTP burn supply / Connect to VLED in normal application
B4	VBUS	PWR	Digital supply voltage / interface voltage. For 1.8V connect to VP18.
B6	SDA	DIO	I²C / I3C data
B8	ID0	DIO	I²C address pin / GPIO
B10	DVSS	PWR	Connect to ground
C1	VLED	PWR	LED supply voltage
C3	EN	DIO	Enable input pin
C5	TEST	DIO	Test enable pin / connect to ground
C7	PVSS	PWR	Power ground / connect to ground
C9	ID1	DIO	I²C address pin / GPIO
C11	AVSS	PWR	Analog ground / connect to ground
D2	LN7	AIO	Current sink input 7 (LED cathode)
D4	LN5	AIO	Current sink input 5 (LED cathode)
D6	LN3	AIO	Current sink input 3 (LED cathode)
D8	LN1	AIO	Current sink input 1 (LED cathode)
D10	VP18	PWR	LDO output. Connect 2.2µF capacitor close to pin VP18.
E1	PVSS	PWR	Power ground / connect to ground
E3	LN6	AIO	Current sink input 6 (LED cathode)
E5	LN4	AIO	Current sink input 4 (LED cathode)
E7	LN2	AIO	Current sink input 2 (LED cathode)
E9	LN0	AIO	Current sink input 0 (LED cathode)
E11	VP2	PWR	LDO Input. Connect 2.2µF capacitor close to pin VP2.

(1) PWR Power Pin
AIO Analog Input & Output
DIO Digital Input & Output
DI Digital Input
DO Digital Output

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS1181

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
V_{LED}	LED supply voltage to ground	-0.3	5.5	V	Referenced to GND
V_{P2}	LDO supply voltage input	-0.3	5.5	V	Referenced to GND
V_{BURN}	VBURN voltage to ground	-0.3	6.5	V	Referenced to GND
I_{SCR}	Input current (latch-up immunity)	± 100		mA	JEDEC JESD78E
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM	± 2000		V	JS-001-2017
ESD_{CDM}	Electrostatic discharge CDM	± 500		V	JS-002-2018
Temperature ranges and storage conditions					
T_A	Ambient temperature	-20	125	°C	
T_{STRG}	Storage temperature range	-40	85	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020(1)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	1			Floor lifetime unlimited

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn).

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 4: Electrical characteristics of AS1181

Symbol	Parameter	Min	Typ	Max	Unit	Comment
Operating conditions						
T_{A_OP}	Ambient temperature operating	-20	25	85	°C	In this range all specified parameters are met
Power supplies and GND						
V_{LED}	LED supply voltage	2.6		5.5	V	
V_{P2}	Supply voltage for LDO	2.0	2.1	5.5	V	If only one supply voltage is available V_{LED} can be connected to V_{P2}
V_{P18}	Output voltage of LDO	1.71	1.8	1.89	V	Supply for analog and digital circuits
V_{BUS}	Supply voltage VBUS	1.08	1.2	1.98	V	Interface voltage. For 1.8V connect to VP18.
$I_{SHUTDOWN}$	Shutdown current when EN = 0			1	µA	
P_{SLEEP}	Sleep power consumption		100	220	µW	
P_{IDLE}	Idle power consumption		1.4	4	mW	
Current sink specifications						
V_{comp}	Compliance / Headroom voltage of current sinks			0.4	V	
I_{MATCH} (1)	Matching between current sinks from -10°C to 85°C T_A	-1.5		1.5	%	
I_{ACC} (2)	Absolute current sink accuracy full range	-2.5		2.5	%	Full current and temp range
I_{RANGE}	Current sink range	0		66	mA	250µA LSB
I_{RES}	Current sink resolution			8	bit	
T_{ON_MIN}	Minimum LED on time	10			µs	
Temperature monitors						
$TEMP_{OT}$	High temperature shutdown			140	°C	
$TEMP_{UT}$	Low temperature shutdown	-20			°C	

Symbol	Parameter	Min	Typ	Max	Unit	Comment
IO parameters						
V_{IL}	Digital input low voltage	0		0.3x VBUS	V	
V_{IH}	Digital input high voltage	0.7x VBUS		1.98	V	
V_{OL}	Digital output low voltage	0		270	mV	I3C mode; IOL = 3mA
V_{OH}	Digital output high voltage	VDD-0.27			V	I3C mode; IOL = 3mA
f_{SCL_I2C}	I²C maximum frequency			1	MHz	
f_{SCL_I3C}	I3C maximum frequency			12.5	MHz	
PWM inputs (3)						
T_{HIGH}	Strobe/PWM high time	20		15000	µs	
T_{LOW}	Strobe/PWM low time	$65+T_{stagger}$			µs	*$T_{stagger}$ - time needed to perform all the staggering for all groups, if staggering is disabled equals to zero.
P_{PWM}	PWM period	0.2		16.6	ms	PWM1 and PWM2 shall have the same period in dual PWM input mode.
f_{PWM}	PWM frequency	60		5000	Hz	
DC	Duty cycle	10		90	%	
t_{skew}	PWM1&2 input skew			10	µs	Maximum skew between PWM1 and PWM2 input in all modes.

(1) Error/current sink mismatch calculated with all channel currents averaged.
(2) Calibrated and measured on every device in final test (ATE). System measurement accuracy and solder shift are not included. Accuracy defined on device level.
(3) Valid in external PWM mode for inputs STROBE1_PWM1 & ID2_PWM2

6 Typical operating characteristics

Figure 3: Dual PWM input, T_STAGGER = 0µs

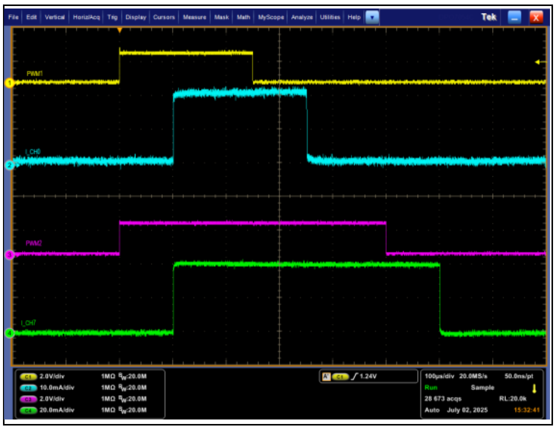
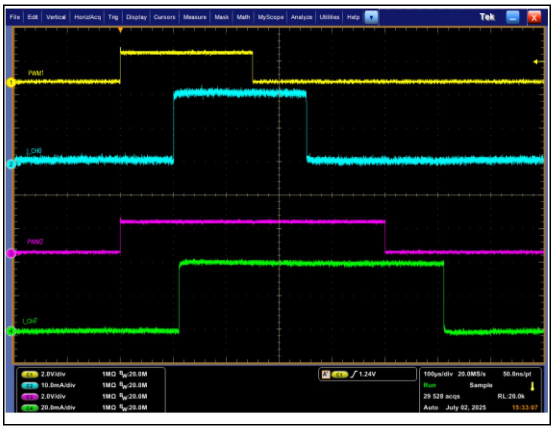


Figure 4: Dual PWM input, T_STAGGER = 10µs



(1) I_CH0 = 20mA; I_CH7 = 40mA

Figure 5: 1 PWM input, T_STAGGER = 1µs

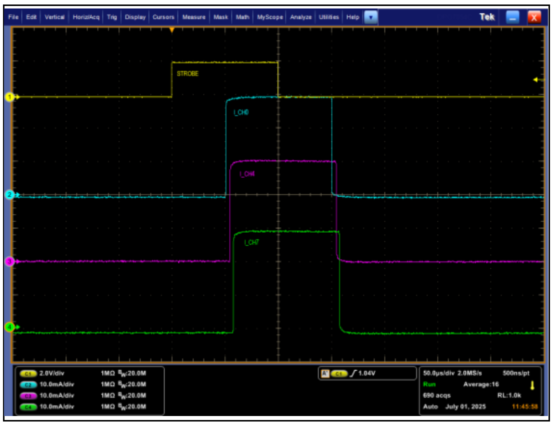
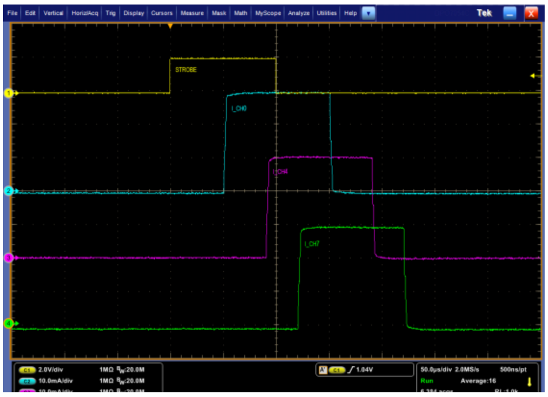


Figure 6: 1 PWM input, T_STAGGER = 10µs

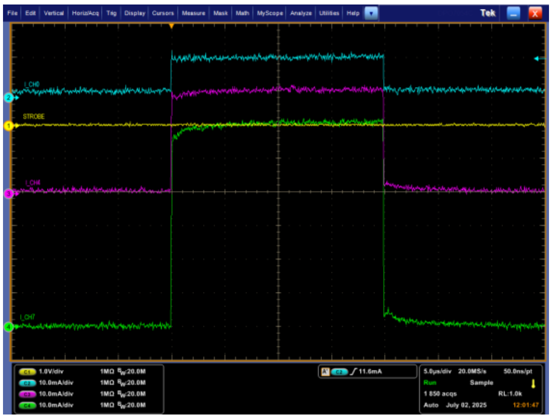
(1) I_CH0, I_CH4, I_CH7 = 30mA

Figure 7: 1 PWM input, T_STAGGER = 1µs



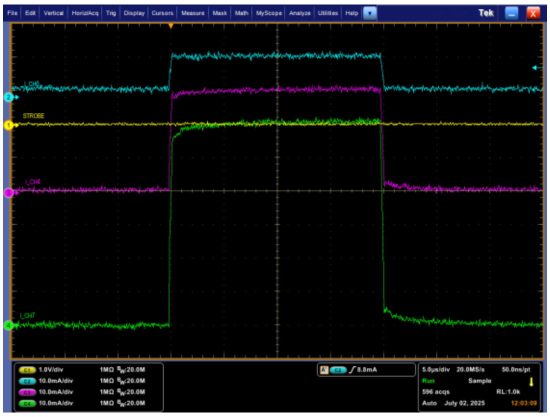
(1) I_CH0, I_CH4, I_CH7 = 30mA
(2) Slew rate = 24 x 4

Figure 8: Current pulse 20µs ON time



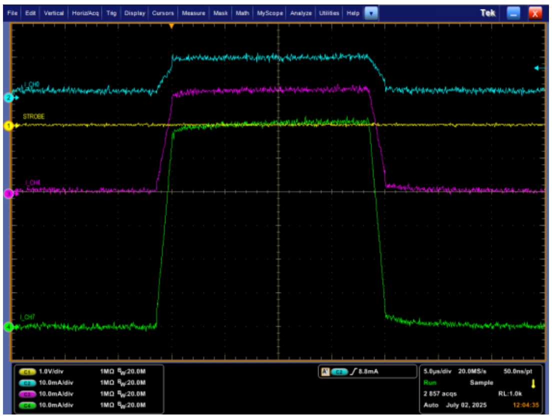
(1) I_CH0 = 10mA, I_CH4 = 20mA, I_CH7 = 60mA
(2) Slew rate = 0x1

Figure 9: Current pulse 20µs ON time



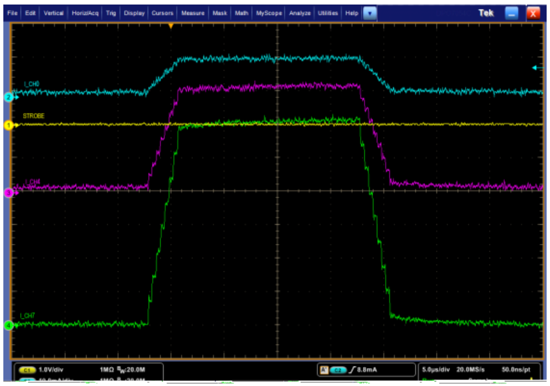
(1) I_CH0 = 10mA, I_CH4 = 20mA, I_CH7 = 60mA
(2) Slew rate = 3x4

Figure 10: Current pulse 20µs ON time



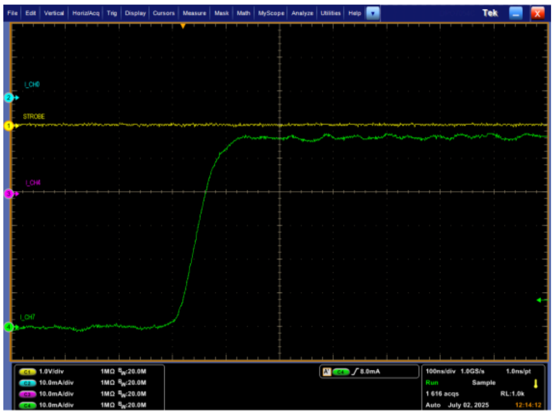
(1) I_CH0 = 10mA, I_CH4 = 20mA, I_CH7 = 60mA
(2) Slew rate = 15 x 6

Figure 11: Current pulse 20µs ON time



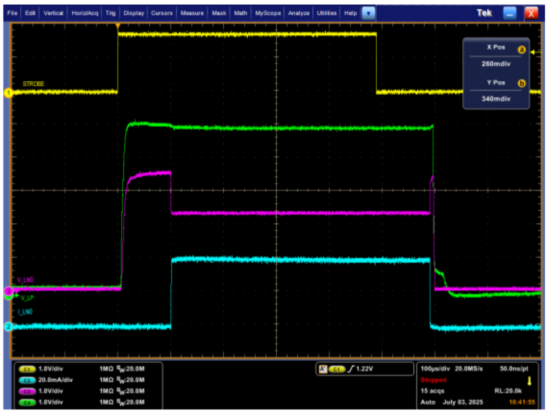
(1) I_CH0 = 10mA, I_CH4 = 20mA, I_CH7 = 60mA
(2) Slew rate = 28 x 8

Figure 12: Current sink rise time



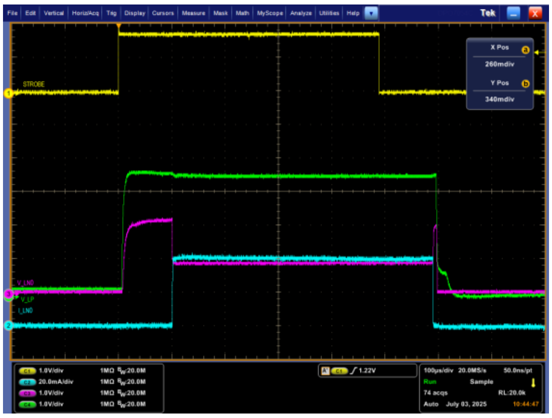
(1) I_CH7 = 60mA
(2) Slew rate = 0

Figure 13: Typical channel enable



(1) V_LP (VLED, green) = 5V; V_LN0 (purple)
(2) I_CH0 (blue) = 40mA

Figure 14: Typical channel enable



(1) V_LP (VLED, green) = 3.6V; V_LN0 (purple)
(2) I_CH0 (blue) = 40mA

Figure 15: Typical channel matching @ 4mA(1)

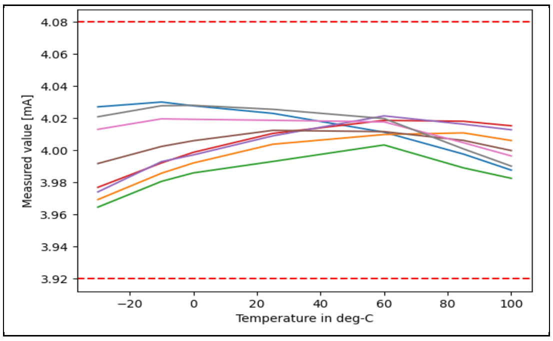
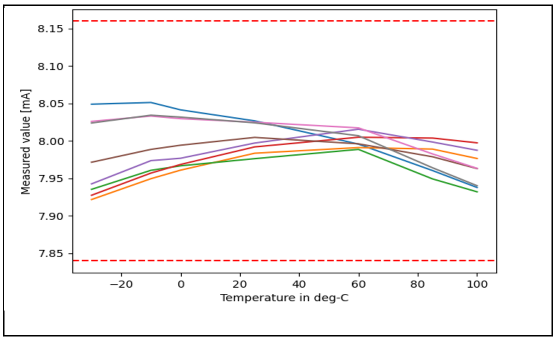


Figure 16: Typical channel matching @ 8mA(1)



(1) Typical Channel (LNx) matching of 1 device over temperature. Individual colored lines represent LNx current/LED current.

Figure 17: Typical channel matching @ 32mA(1)

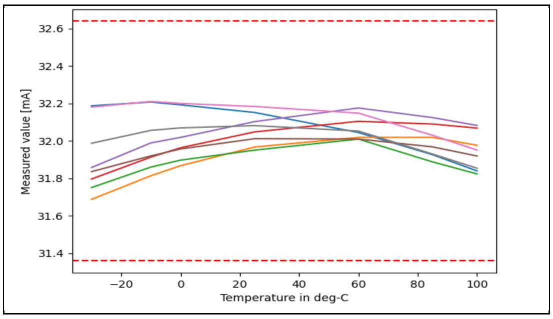
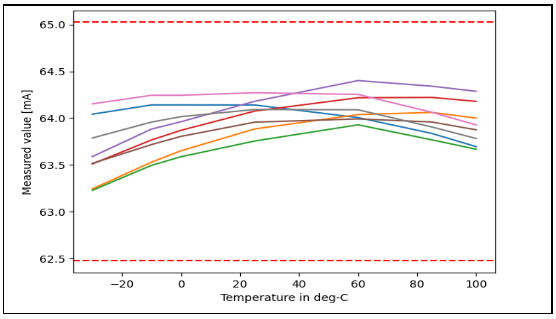


Figure 18: Typical channel matching @ 64mA(1)

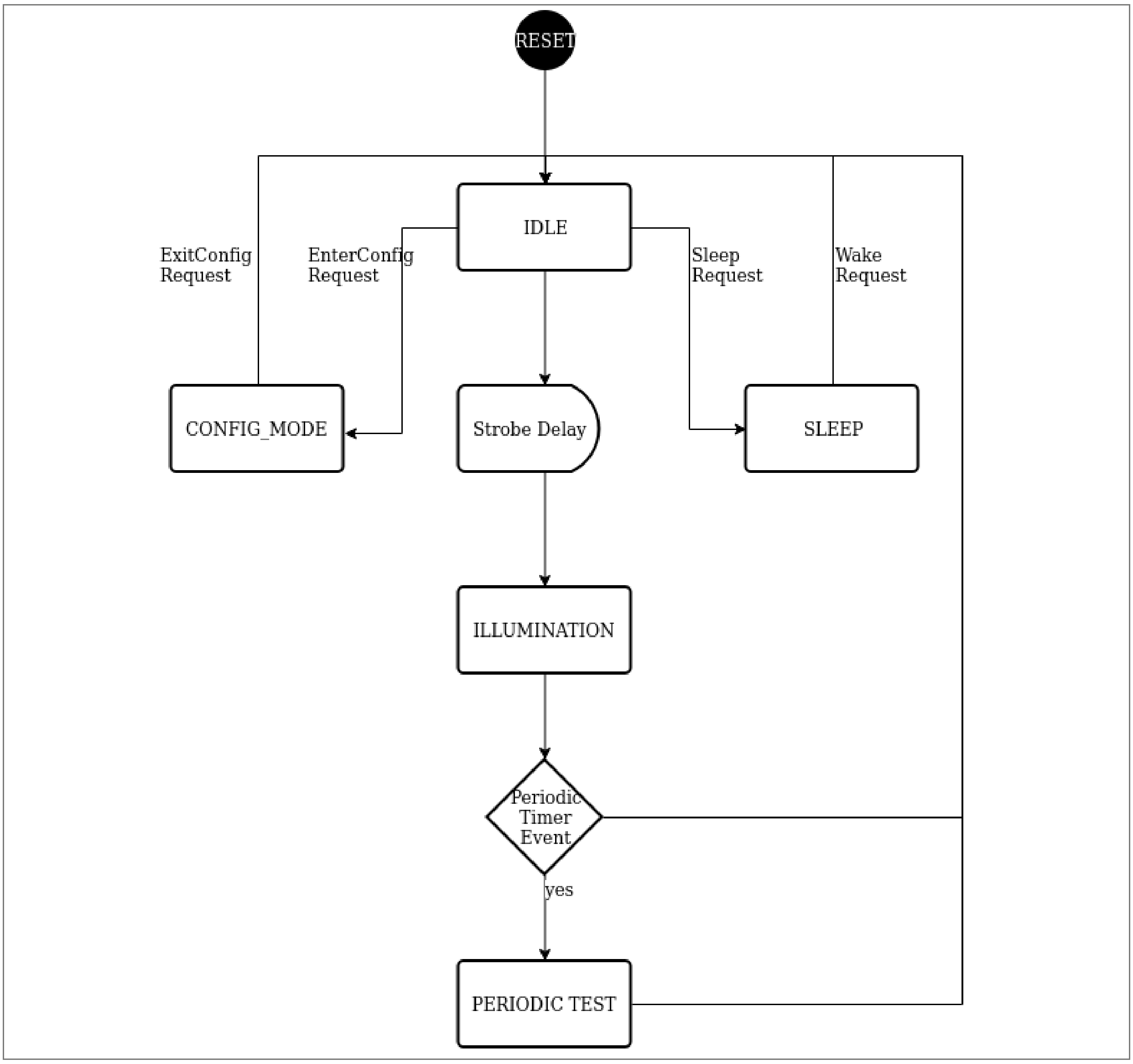


(1) Typical Channel (LNx) matching of 1 device over temperature. Individual colored lines represent LNx current/LED current.

7 Functional description

7.1 Operation modes

Figure 19: Operation modes flow diagram



7.1.1 Sleep mode

The Sleep mode can be entered by writing the SLEEP command to the I2C_COMMAND_CODE register (in I²C mode) or by executing the CCC SLEEP (in I3C mode).

The Sleep mode can only be left by writing the WAKE command to the I2C_COMMAND_CODE register (in I²C mode) or by executing the CCC WAKE (in I3C mode).

During Sleep mode the following register access is possible:

- Writing to I2C_COMMAND_CODE register
- Reading SYSTEM_STATE register
- All other writes to any address don't take any effect
- All other reads to any address return 0xFFFF

When the device uses I3C the following direct and indirect CCC operations are possible, with the following exceptions:

- ENEC/DISEC will only take effect after WAKE has been sent
- CCC Strobe, ClearIRQ, and RunSelfTest don't trigger any CPU task
- IBI generation and IRQ_N assertion is delayed by the oscillator start time

7.1.2 Config mode

Safety relevant registers can only be changed from I3C when the “config_mode” bit is set. Within this mode, no new illumination cycle is allowed to happen.

Entering this mode is protected by a 32-bit key which is stored in CONFIG_KEY_COMP register. Before sending the change mode CCC, the register CONFIG_KEY needs to contain the same key as CONFIG_KEY_COMP in order to toggle the config_mode bit. The CONFIG_KEY registers get cleared to 0 on each try to toggle the config_mode bit.

This means that before entering and before exiting the config mode, the specific key needs to be stored in the CONFIG_KEY registers.

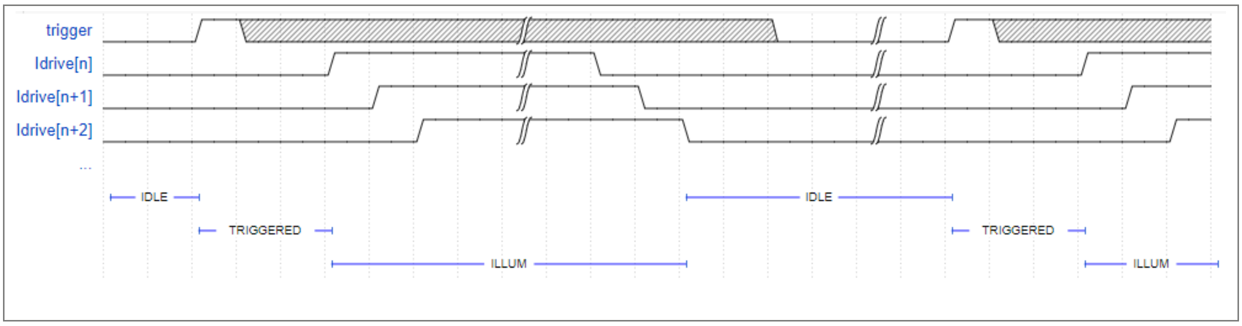
7.1.3 Illumination sequence & STROBE mode

The illumination sequence always starts in IDLE state when a strobe is asserted.

The strobe will enter state "TRIGGERED" depending on the strobe delay defined in CH_DLY register (Address 0x1A24) bit "TD_TRIGDLY" or skip this state when TD_TRIGDLY is "0".

The state ILLUM lasts from the first channel that is turned on to the last channel that is turned off. In STROBE mode the illumination duration is defined internally by the TD_ILLUM register (Address 0x1A00).

Figure 20: Illumination sequence



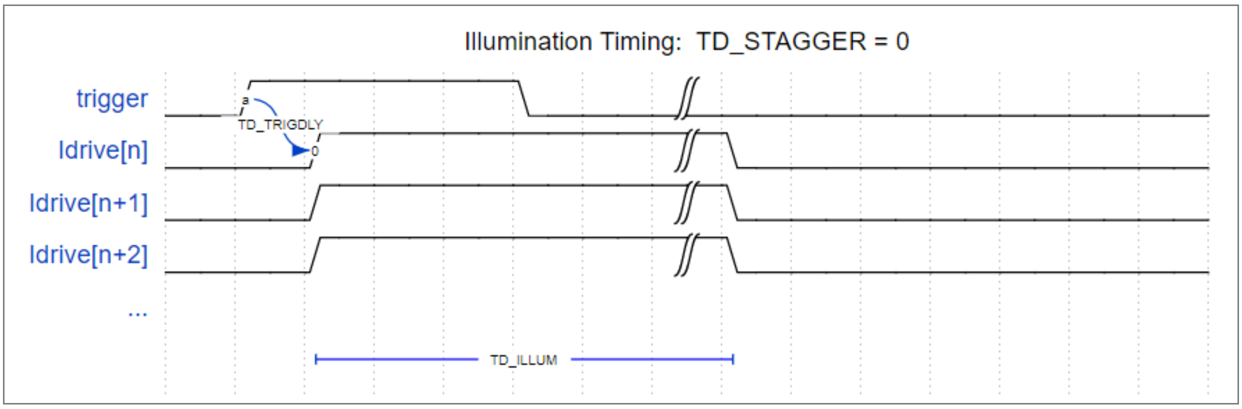
7.1.3.1 Stagger delay

Stagger delay is controlled by CH_DLY register (Address 0x1A24) bit "TD_STAGGER" and allows to add a delay before the next channel group is turned on/off.

Information:

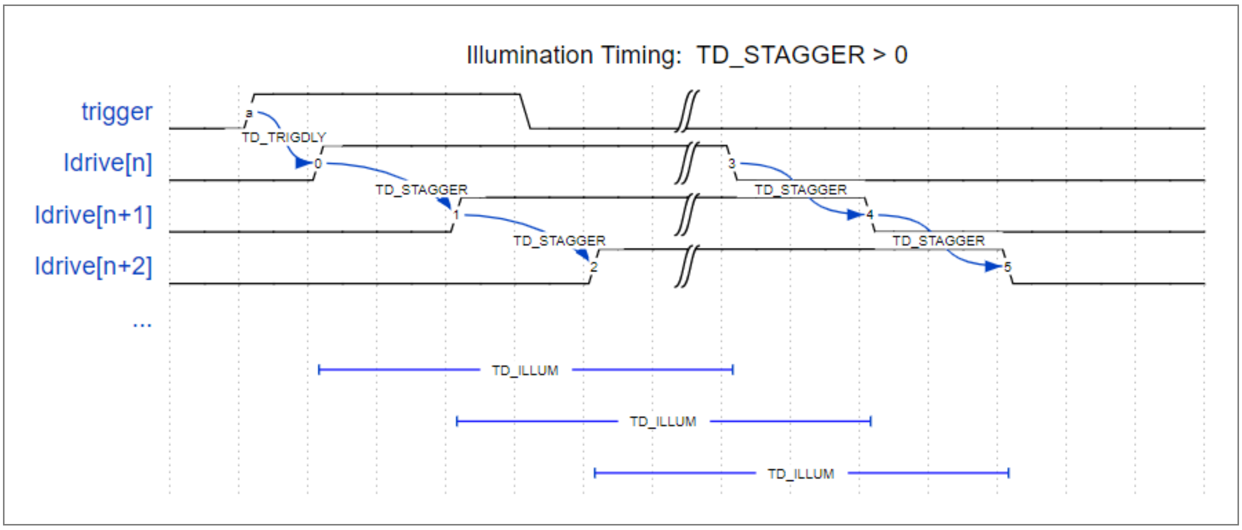
A group can contain 1 or more channels.

Figure 21: TD_STAGGER = 0



(1) TD_STAGGER = 0: All channels are turned on at the same time.

Figure 22: TD_STAGGER > 0



The channels turn on one by one, each delayed by TD_STAGGER. The channel with the lowest number will turn on first.

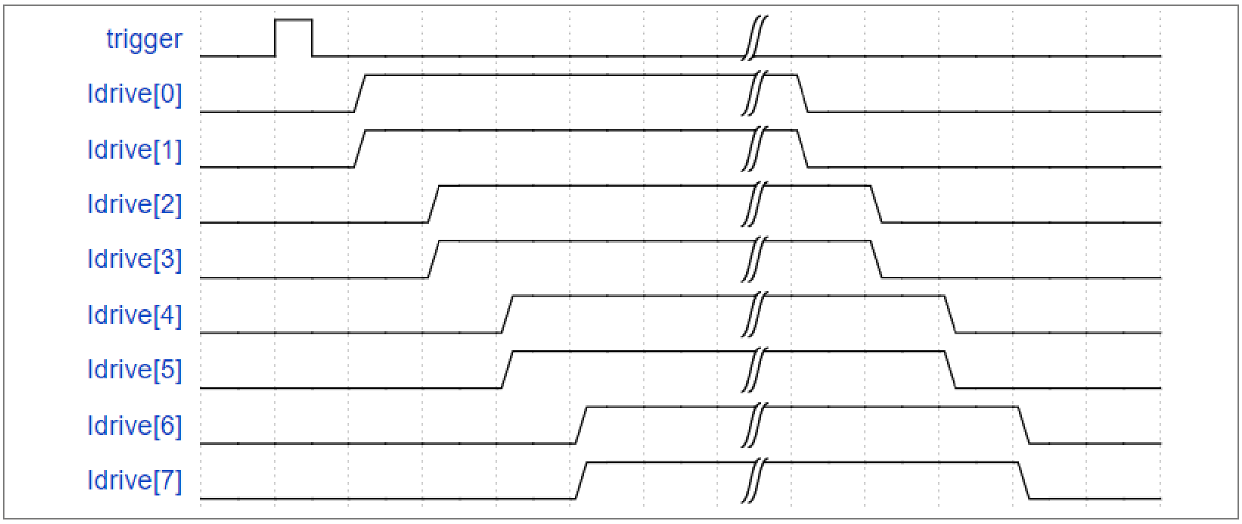
7.1.4 Channel grouping

Grouping is defined by the CH_GROUP register (Address 0x1A22) and CH_ENABLE register (Address 0x1A26). Channels that are turned off will be skipped and will not add a stagger delay.

The examples below illustrate some channel grouping schemes.

7.1.4.1 Example: CHAN_GROUP is 0x155 & CHAN_ENABLE is 0x3FF

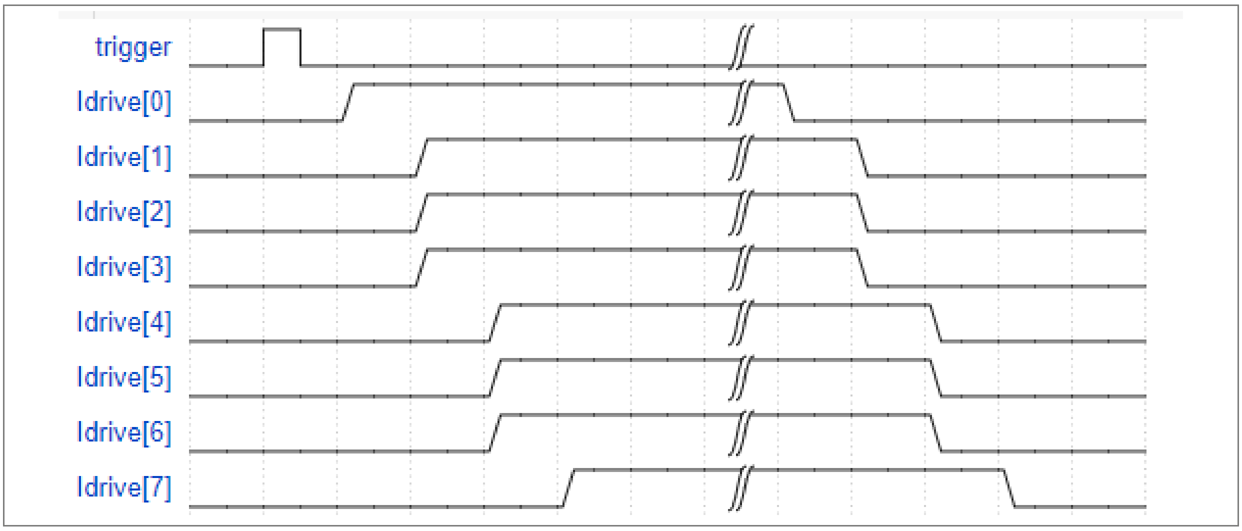
Figure 23: Channel group example 1



(1) Channel groups are 0+1, 2+3, 4+5, 6+7

7.1.4.2 Example: CHAN_GROUP is 0x93 & CHAN_ENABLE is 0x3FF

Figure 24: Channel group example 2

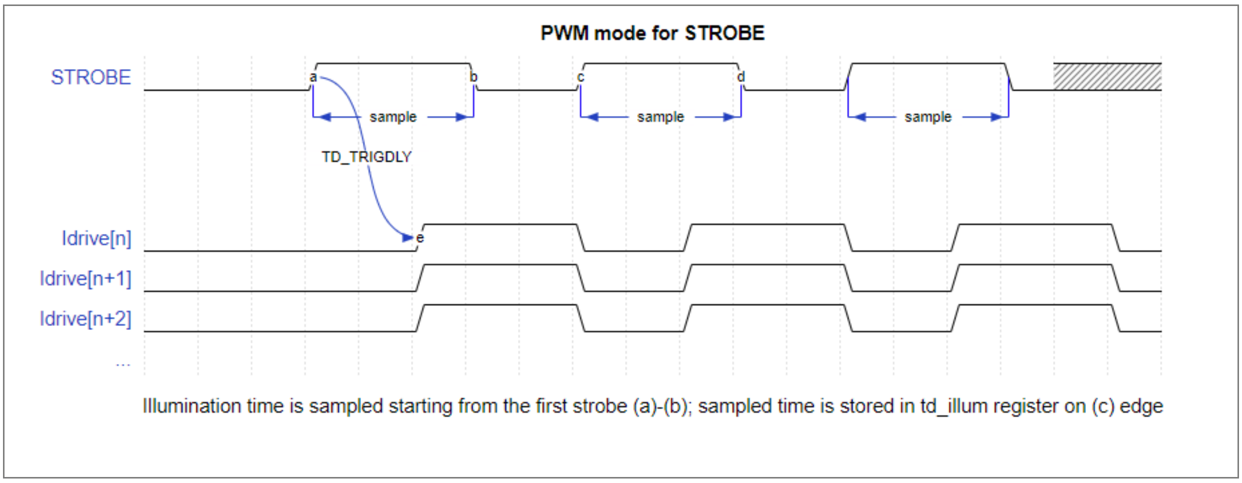


(1) Channel groups are 0, 1+2+3, 4+5+6, 7

7.1.5 Direct PWM mode (1 PWM input)

In direct PWM mode the illumination duration can be controlled by “STROBE1_PWM1” input used as a direct PWM source. If enabled by the PWM_CTR register (Address 0x1A32) bit “*pwm_illum_enable”* the “STROBE1_PWM1” signal on-time determines the illumination duration. Additionally, “TD_ILLUM register (Address 0x1A00) shows sampled illumination duration. Illumination is still triggered by the rising edge of “STROBE1_PWM1” signal, with latency defined in CH_DLY register (Address 0x1A24) bit “TD_TRIGDLY”.

Figure 25: External PWM mode 1



Sampling is continuous and the illumination duration follows the on-time of the “STROBE1_PWM1” signal with *TD_TRIGDLY* latency.

TD_ILLUM register (Address 0x1A00) is updated with newly sampled duration with latency of the one PWM cycle.

Figure 26: Illumination time register update

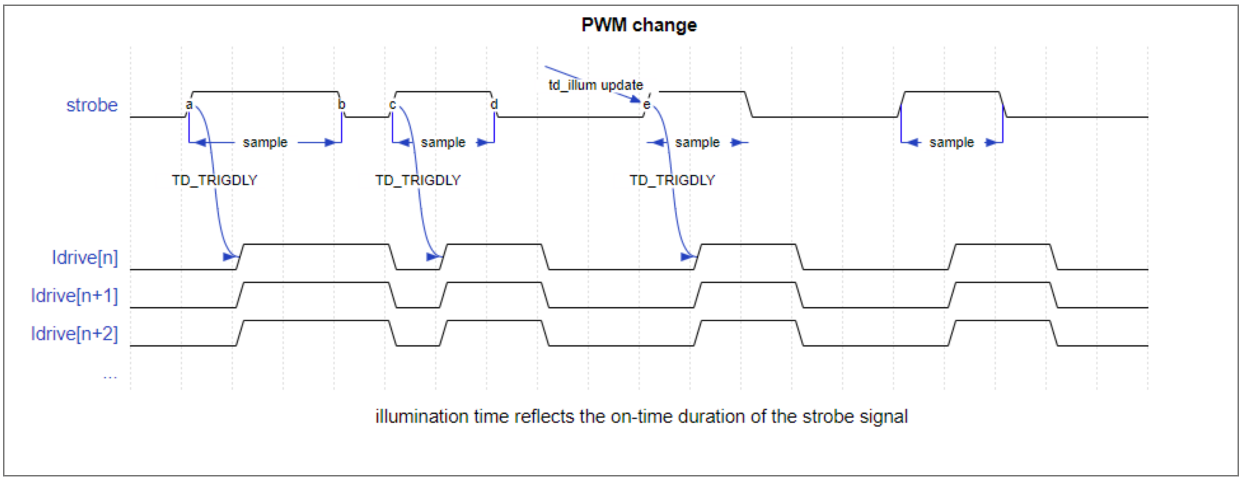
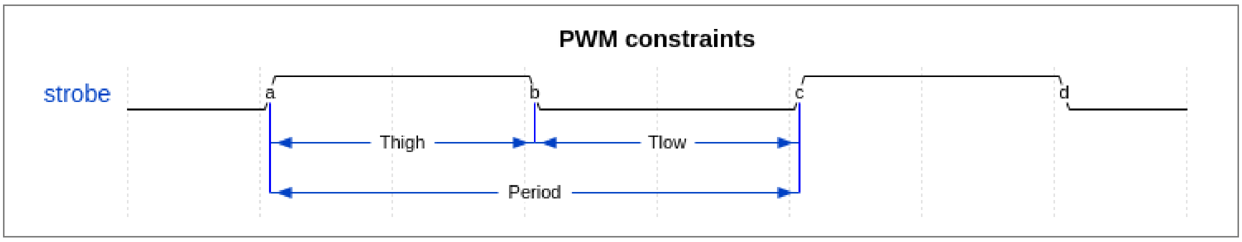


Table 5: External PWM mode constraints

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{HIGH}	Strobe high time	20		15000	µs	
T_{LOW}	Strobe low time	65+Tstagger*			µs	*Tstagger - time needed to perform all the staggering for all groups, if staggering is disabled equals to zero.
P	PWM period	0.2		16.6	ms	PWM1 and PWM2 shall have the same period in dual PWM input mode.
F	PWM frequency	60		5000	Hz	
DC	Duty cycle	10		90	%	
T_{skew}	PWM1&2 input skew			10	µs	Maximum skew between PWM1 and PWM2 input in all modes.

Figure 27: External PWM constraints



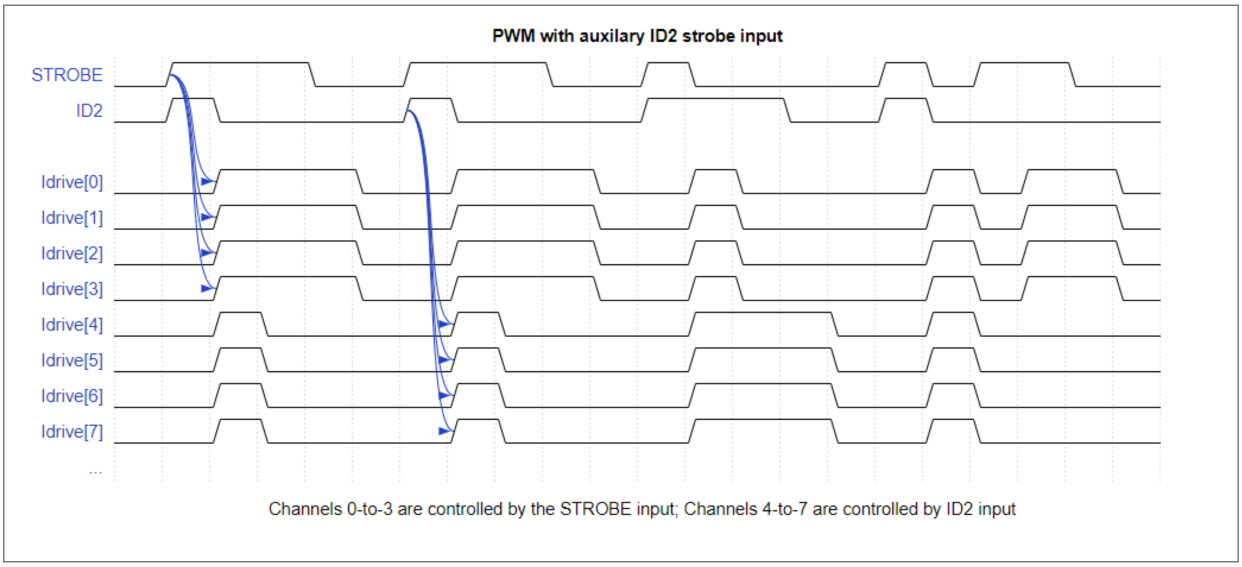
7.1.6 Direct PWM mode (2 PWM inputs)

Illumination duration for channels in PWM Mode can also be controlled by the ID2_PWM2 input, which can be used as 2nd PWM input signal.

The mode is enabled by setting pwm_grp_split field in the PWM_CTR register (Address 0x1A32) to the non-zero value.

The value in the field pwm_grp_split is used to split the channels into two groups. The illumination duration for the channels in the first group is controlled then by the STROBE1_PWM1 input. The illumination duration for the channels in the second group is controlled by the ID2_PWM2 input.

Figure 28: External PWM mode with 2 inputs (dual trigger)



7.1.6.1 Trigger adjustment for the PWM mode with 2 strobe inputs

In default case the illumination sequence is triggered by the first rising edge of either input. The triggering moment can be adjusted by setting the pwm_trig field in the PWM_CTR register (Address 0x1A32) to non-zero value.

- 0x0 – Default, STROBE_PWM1 or ID2_PWM2: Illumination is triggered by the first rising edge of either signal.
- 0x1 – STROBE_PWM1 and ID2_PWM: Illumination is triggered in the moment both signals become high.
- 0x2 – STROBE_PWM1 only: Illumination for both groups is triggered by the rising edge of STROBE_PWM1 input.
- 0x3 – AUX only: Illumination for both groups is triggered by the ID2_PWM2 signal rising edge.

The skew between the rising edges of both inputs in all cases shall be less than 10µs.

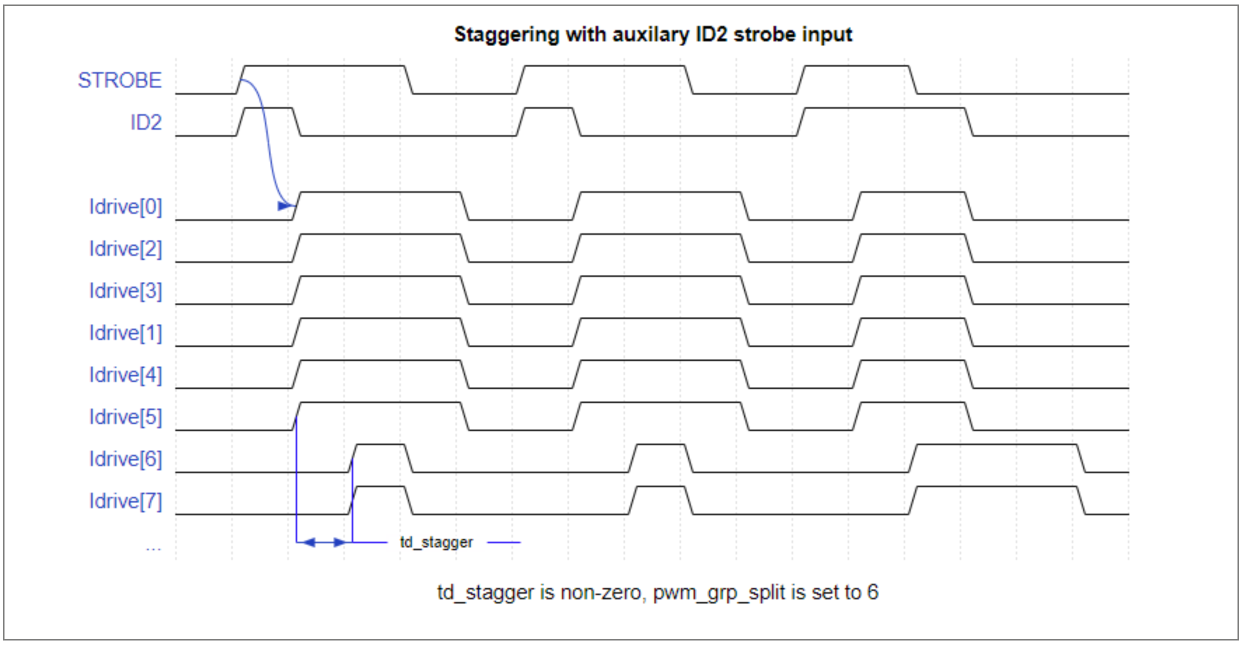
If the other signal edge doesn't come within the skew window, the illumination sequence for this channels group won't start on this cycle.

7.1.6.2 Staggering for the PWM mode with 2 PWM inputs

If “*td_stagger”* field in register CH_DLY register (Address 0x1A24) is set to non-zero value, it applies as a delay in the illumination between channels group assigned to the STROBE_PWM1 input and a group assigned to the ID2_PWM2 input.

Note that in this mode the grouping defined in the CH_GROUP register (Address 0x1A22) is ignored, the grouping follows “*pwm_grp_split”* field setting in register PWM_CTR register (Address 0x1A32).

Figure 29: Stagger delay with 2 external PWM inputs

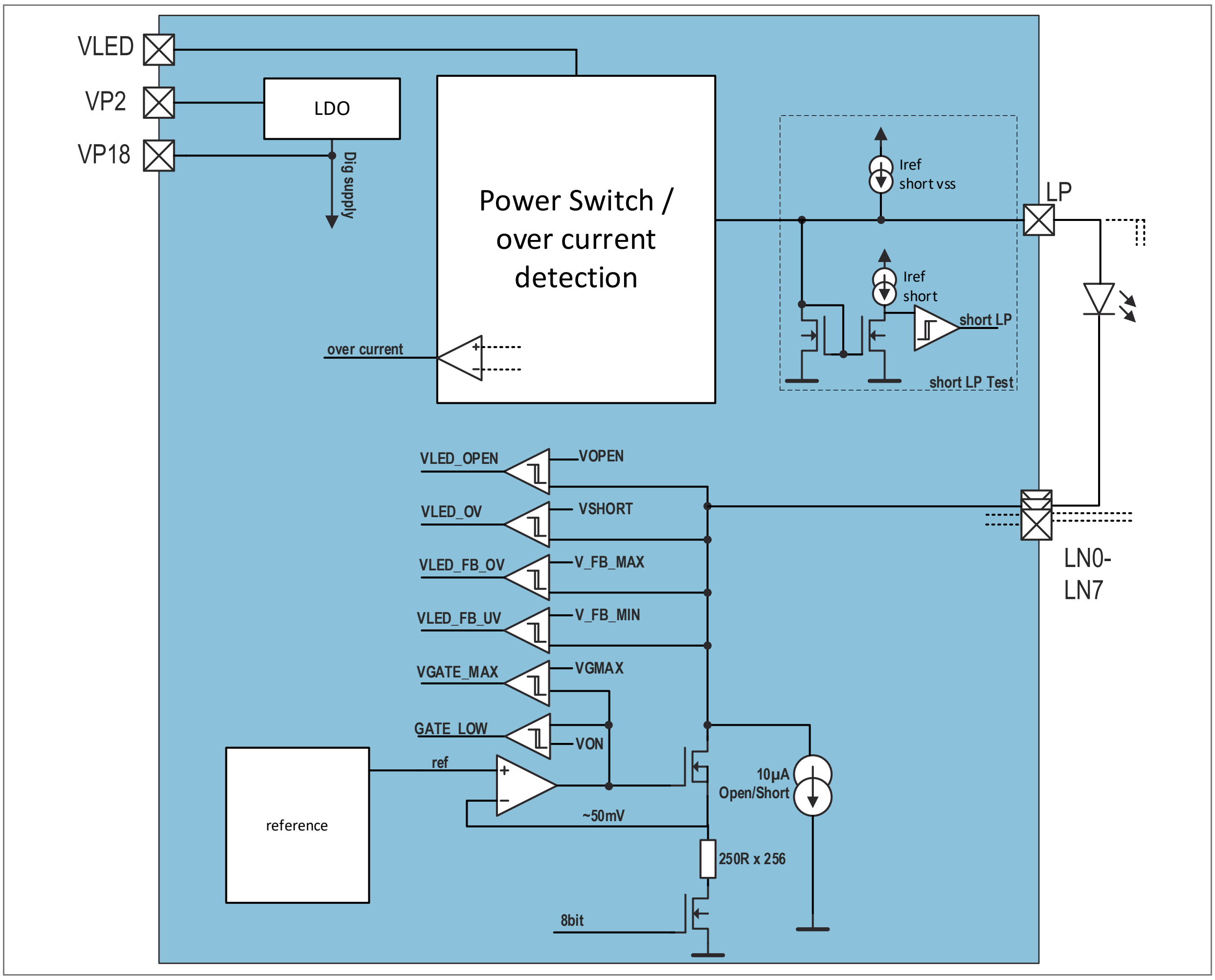


7.2 Safety monitors

AS1181 integrates several safety features to detect open or shorted LEDs and to avoid unwanted overcurrent situations also under single fault conditions.

Safety features are implemented on the high side (LP - Anode) and low side (LNx - Cathode) of the LEDs as shown in the detailed block diagram below. All safety features are operating fully self-contained and do not require an external host to shut down illumination.

Figure 30: Block diagram safety monitors



7.2.1 High side safety monitors

7.2.1.1 Power switch / overcurrent detection

The current applied to the LEDs is measured and compared to an internal reference current in the high side current path (LP node). This reference current defines the turn off threshold and can be programmed in HSCS_SEL register (Address 0x1A30). The individual channel current limits can be defined in CURR_LIM0 register (Address 0x1A12) to CURR_LIM7 register (Address 0x1A20).

7.2.1.2 LP node open/short detection

LP shorts and open (anode connection of the LED) are detected using current sources in the “short LP” section of Figure 26 while the power switch is off to prevent accidental illumination or uncontrolled current paths outside the LEDs.

7.2.2 Low side safety monitors

7.2.2.1 Open and short LED detection

Checks for open and shorted LEDs are done at the cathode connection (LNx) of the LEDs. If the voltage on the LNx pin is higher than a programmed threshold voltage a shorted LED is detected and if the voltage on the LNx pin is lower than a programmed threshold open LEDs are detected. The detection thresholds are pre-programed in OTP and can be adjusted in the COMP_LVL_SHORT register (Address 0x1A4C) and COMP_LVL_OPEN register (Address 0x1A4E).

7.2.3 Digital safety monitors

7.2.3.1 Illumination time monitor

The illumination time monitor is continuously sampling the PWM ON time applied via both inputs and comparing the result with the value programed in “TD_ILLUM_MAX register (Address 0x1A36)”. In PWM mode the ON time (HIGH Time) is constrained to be maximum 15ms. Therefore, the value in the TD_ILLUM_MAX register shall be less the 15ms in this mode. (Refer to Table 5: External PWM mode constraints).

If the actual PWM ON time is longer than the value programmed the current sinks get turned off and the respective interrupt flag is set.

Figure 27 shows the actual implementation – in the 3rd frame (STROBE = yellow) the PWM ON time changes from 4ms to 10ms – TD_ILLUM_MAX is programed to 4.1ms.

The current sink (blue) is turned off immediately and the interrupt IRQ_N (green) is pulled to GND. The interrupt “Illumination Duration” has been set and is informing the Host.

Figure 31: Illumination time monitor example

7.2.3.2 Strobe rate monitor in STROBE mode

The strobe rate monitor measures the applied strobe signal frequency and compares it to the value stored in TD_TRATE_MAX register (Address 0x1A34). If the applied strobe signal is too fast, an interrupt is set to inform the host. Note that the strobe rate monitor is not available in direct PWM mode with 1 or 2 inputs.

7.2.4 BIST (Built-in-self test)

A built-in-self test is implemented periodically check the device safety monitors.

After power-on-reset the digital BIST is checking RAM, ROM and OTP followed by the analog BIST checking the following circuits:

1. VLED voltage monitor and error injection to test comparator toggling.
2. VP18 voltage monitor and error injection to test comparator toggling.
3. Temperature monitor and error injection to test comparator toggling.
4. LN shorts and open tests.
5. LN comparator and error injection to test comparator toggling.
6. LP shorts and open tests.
7. LP comparator error and error injection to test comparator toggling.
8. High-side power switch / Overcurrent detection" circuit operation.

Note: Error injection tests are done after power on-reset only while LNx & LP short/open tests are done continuously.

7.2.5 Temperature shutdown

The device integrates an on-chip temperature supervision for over and under temperature situations. If the device is exposed to too high or too low temperatures it will shut down the current sinks, sets respective interrupt and informs the host.

7.3 Interrupt controller

Interrupt requests are sent to output pin IRQ_N. This signal is active low and the pin is configured as open drain output.

The condition to trigger an interrupt for a specific source is:

- If an interrupt source is ASSERTED, ENABLED and NOT MASKED, then the IRQ_N is asserted.
- If an interrupt source is asserted, then it is captured in the interrupt status register IRQ_STATUS0 register (Address 0x1AA4), IRQ_STATUS1 register (Address 0x1AA6) and IRQ_STATUS2 register (Address 0x1AA8).
- An interrupt is enabled if the corresponding enable register bit is set to 1 in the following registers: IRQ_ENABLE0 register (Address 0x1A38), IRQ_ENABLE1 register (Address 0x1A3A) and IRQ_ENABLE2 register (Address 0x1A3C).
- An interrupt can be masked(inhibited) if the corresponding mask register bit is set to 1 in the following registers: IRQ_MASK0 register (Address 0x1AB0), IRQ_MASK1 register (Address 0x1AB2), IRQ_MASK2 register (Address 0x1AB4).
- IRQ_N is latched on the first interrupt occurrence.
- IRQ_N is not cleared until all interrupt status registers containing a set interrupt are read (reading the interrupt status registers clears them).
- The IRQ_N output signal is the NOR-function of all interrupt sources.

7.3.1 Interrupt sources

AS1181 has the following interrupt sources:

Interrupts 0-15 can be managed with the following registers:

- IRQ_ENABLE0 register (Address 0x1A38)
- IRQ_STATUS0 register (Address 0x1AA4)
- IRQ_HISTORY0 register (Address 0x1AAA)
- IRQ_MASK0 register (Address 0x1AB0)

Table 6: Interrupt sources 0-15

Bit	Source	Severity	Interrupt type	Description
0	fault	Highest	Pulse/level	System fault (asserted by safety monitor) (The OR-function of all ‘critical’ errors)
1	fv_tc_done	Info	Pulse	Temperature compensation completed
2	vload_adj_request	Info	Pulse	Vload adjust request – set when idrive_undervoltage is asserted
3	asic_test_done	Info	Pulse	RunSelfTest completed
4	boot_complete	Info	Pulse	Startup(Boot) completed
5	task_done	Info	Pulse	Task done
6	periodic_test_done	Info	Pulse	Periodic test done (“max_timer”)
7	illum_start	Info	Pulse	Illumination start of first channel
8	illum_end	Info	Pulse	Illumination end of last channel
9	over_temp	Critical	Level	Over temperature (temp. > 125deg)
10	idrive_overvoltage	Info	Pulse	Overvoltage on any active channel
11	idrive_undervoltage	Info	Pulse	Undervoltage on any active channel
12	trigger_rate_error	Critical	Pulse	Trigger rate check (“min_timer”)
13	ecc_error	Critical	Level	OTP ECC error
14	idrive_ramp_error	Critical	Pulse	Channel Ramp-down error
15	illum_duration_error	Critical	Pulse	Illumination time error

Interrupts 16-31 can be managed with the following registers:

- IRQ_ENABLE1 register (Address 0x1A3A)
- IRQ_STATUS1 register (Address 0x1AA6)
- IRQ_HISTORY1 register (Address 0x1AAC)
- IRQ_MASK1 register (Address 0x1AB2)

Table 7: Interrupt sources 16-31

Bit	Source	Severity	Interrupt type	Description
0	osc_error	Critical	Pulse	Oscillator period error
1	watchdog_timeout	Critical	Pulse	Watchdog timeout error
2	rload_test_error	Critical	Pulse	Rload test failure
3	hs_overcurrent	Critical	Pulse/ level	HS switch overcurrent error (BIST & continuous check)
4	curr_lim_hi_overrun	Critical	Level	Overcurrent error on any channel
5	curr_lim_lo_underrun	Critical	Level	Undercurrent error on any channel
6	supply_overvoltage	Critical	Level	Overvoltage error on VP18 or Vload
7	supply_undervoltage	Critical	Level	Undervoltage error on VP18 or Vload
8	lp_short_open_error	Critical	Pulse/ level	LP short or open failure (BIST & continuous check)
9	ln_short_open_error	Critical	Pulse/ level	LN short or open failure (BIST & continuous check)
10	idrive_feedback_error	Critical	Level	idrive vs. analog current comparison failure
11	otp_test	Critical	Pulse	OTP read check error
12	ram_bist	Critical	Pulse	RAM BIST error
13	rom_bist	Critical	Pulse	ROM BIST error
14	Not used			
15	Not used			

Interrupts 32-38 can be managed with the following registers:

- IRQ_ENABLE2 register (Address 0x1A3C)
- IRQ_STATUS2 register (Address 0x1AA8)
- IRQ_HISTORY2 register (Address 0x1AAE)
- IRQ_MASK2 register (Address 0x1AB4)

Table 8: Interrupt sources 32-38

Bit	Source	Severity	Interrupt type	Description
0	vload_monitor_error	Critical	Pulse	VLOAD BIST fail
1	vp18_monitor_error	Critical	Pulse	VP18 BIST fail
2	temp_detect_error	Critical	Pulse	Temperature BIST fail
3	adc_bist_error	Critical	Pulse	ADC BIST fail
4	ls_overcurrent	Critical	Level	vgate_low
5	driver_gate_short	Critical	Level	driver_gate_max on
6	ldo_overcurrent	Critical	Level	LDO overcurrent

7.3.2 Interrupt status & history

Reading the 3 “IRQ_STATUS” registers will automatically clear the corresponding interrupt status bits.

Before clearing is done, the contents of “IRQ_STATUS” are copied into register IRQ_HISTORY0 register (Address 0x1AAA), IRQ_HISTORY1 register (Address 0x1AAC) and IRQ_HISTORY2 register (Address 0x1AAE) to backup the interrupt status.

The interrupt output signal IRQ_N will be de-asserted only after the 3 status registers have been read.

The I3C CCC command 'ClearFaults' clears all status bits in IRQ_STATUS0 to IRQ_STATUS3 with one exception IRQ_STATUS[0] (bit 0, “fault”) will only be cleared with I3C CCC command 'Reset'.

Note: Only interrupt status bits of type 'pulse' (see Table 6, Table 7, Table 8) will be cleared immediately. Interrupt status bits of interrupts with type 'level' will be cleared after interrupt source has vanished.

7.4 Serial interface description (I²C and I3C)

The device supports both I²C and I3C interface. The I3C Target is implemented according to the MIPI-I3C Basic specification v1.1.1. The Target module is connected as a master on the internal system bus.

The default communication mode for AS1181 is I²C, where no in-band interrupts are generated. In the I²C mode 50ns spike filters in the pad cells are enabled.

The I²C spike filter in the pads get disabled after I3C communication is detected in the address header (header needs to be transported with I²C timings).

In-Band-Interrupts are initially disabled and need to be enabled with the ENEC CCC.

I²C is supported up to 1Mbps (fast mode plus).

7.4.1 Operation in legacy I²C mode

I3C CCC messages are not supported in I²C systems, there are the following limitations:

- Broadcast Strobe can be initiated by the external signal or by writing the Strobe command code to the I2C_COMMAND_CODE register.
- Interrupts are only asserted on output pin IRQ_N

7.4.2 I3C supported features

Table 9: I3C feature support

Feature	Supported
Single Data Rate (SDR) messaging mode up to 12.5 MHz	Yes
High Data Rate (HDR) messaging modes	No
Dynamic Address Assignment (DAA)	Yes
Request In-Band Interrupts	Yes
Generate Hot-Join events	No
Controller device capability	No
Legacy I²C messaging	Yes
Timing control	No

7.4.3 I3C CCC commands

I3C devices according to MIPI specification support various common command codes (CCC) to control certain features of the device.

Following Broadcast and Direct Vendor Common Command Codes (VCCCs) are defined specifically for AS1181. There is no payload byte on any of the VCCCs.

Table 10: I3C CCC commands

Name	Broadcast code	Direct code	Description
Reset	0x61	0xE1	Resets the device.
Strobe	0x62	0xE2	Initiates an illumination sequence and is the equivalent of asserting the hardware strobe input signal.
ClearIRQ	0x63	0xE3	Clears all IRQ_STATUS registers. This can be used after an IBI-Request has been acknowledged.
Sleep	0x64	0xE4	Sends the device from IDLE into SLEEP state. I3C target remains powered enabling the subsequent commands to be processed, use the Wake CCC to wake the device from SLEEP state.
Wake	0x65	0xE5	Wake the device from internal SLEEP state to IDLE state.
ChangeMode	0x66	0xE6	Compares the content of CONFIG_KEY registers with CONFIG_KEY_COMP and toggles the config_mode bit on a match. CONFIG_KEY will always be cleared after the compare is done.
Do not use	*0x67*	*0xE7*	
AnalogSelfTest	0x68	0xE8	Executes all analog BISTs which are also executed during startup.
PeriodicTest	0x69	0xE9	Executes the periodic test sequences.
Do not use	0x6A	0xEA	
DigitalSelfTest	0x6B	0xEB	Executes all digital BISTs which are also executed during startup.
Do not use	*0x6C - 0x6F*	*0xEC - 0xEF*	
Do not use	*0x70*	*0xF0*	
Do not use	*0x71*	*0xF1*	
VfMeasurement	0x72	0xF2	Runs a VF Measurement on a selected channel. Can only be executed in CONFIG_MODE.
Do not use	0x73 - 0x77	0xF3 - 0xF7	
Do not use	0x78 - 0x7E	0xF8 - 0xFE	
Do not use	0x7F	-	

Note: After a direct CCC has been sent to the device a STOP condition needs to follow before the next CCC can be sent.

7.4.4 Dynamically assigned addresses

The device supports I3C Dynamic Address Assignment, which is initiated by the external host controller with the broadcast common command code 'Enter Dynamic Address Assignment' (ENTDAA).

The device supports Dynamic Address Assignment in the condition where the external host can overwrite the device statically assigned address using the common command code 'Set Dynamic Address from Static Address' (SETDASA).

After an address is dynamically assigned, the device only responds to the newly assigned address and no longer responds to the default target address. The dynamically assigned address shall be used until the device is reset, at which point the device shall return to its default target address.

7.4.5 Default I²C and I3C slave address

The default 7-bit I²C / I3C address is defined as follows. The ID1 and ID0 are input pins of the device.

Table 11: Serial interface slave address configuration

A6	A5	A4	A3	A2	A1	A0
1	0	1	0	0	**ID1**	**ID0**

Note that the I²C / I3C static address space is from **50h to 53h** depending on the input levels of ID1 and ID0.

7.4.6 I²C read & write command

Figure 32: I²C write data

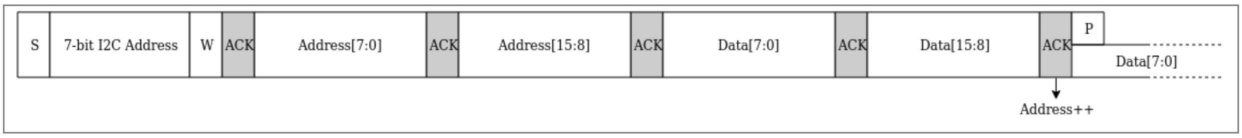
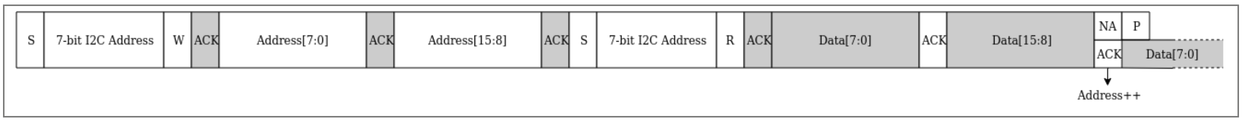


Figure 33: I²C read data



7.4.7 I3C read & write command

Figure 34: I3C private write data

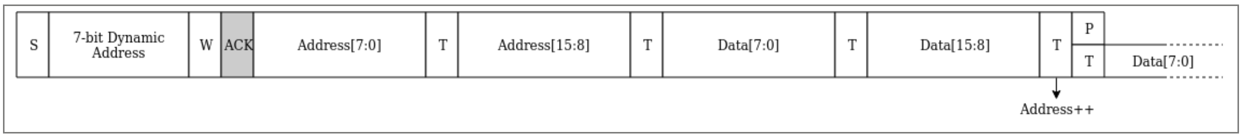
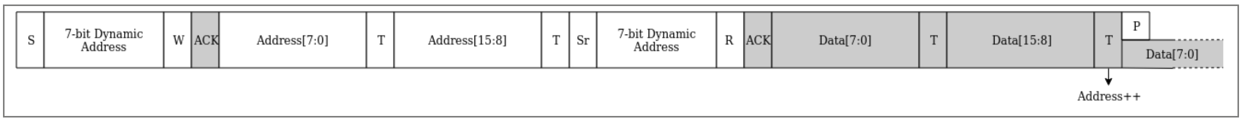


Figure 35: I3C private read data



8 Register description

8.1 Detailed register description

8.1.1 TD_ILLUM register (Address 0x1A00)

Table 12: TD_ILLUM register (Write Access when system state == idle)

Addr: 0x1A00		TD_ILLUM		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
10:0	*td_illum*	0x0	RW	LED illumination duration defined in [µs]. **Note:** If pwm_illum_enable is high this field shows sampled illumination time based on STROBE pin as a PWM source. In pwm mode h'7fff sampled value means constant high STROBE input and constant illumination.

8.1.2 CURR0 register (Address 0x1A02)

Table 13: CURR0 register (Write Access when system state == idle)

Addr: 0x1A02		CURR0		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*curr0*	0x0	RW	LED current for channel 0. Used for internal sensing. 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*
15:8	*curr0_target*	0x0	RW	Target LED current for channel 0 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*

8.1.3 CURR1 register (Address 0x1A04)

Table 14: CURR1 register (Write Access when system state == idle)

Addr: 0x1A04		CURR1		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*curr1*	0x0	RW	LED current for channel 1. Used for internal sensing. 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*
15:8	*curr1_target*	0x0	RW	Target LED current for channel 1 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*

8.1.4 CURR2 register (Address 0x1A06)

Table 15: CURR2 register (Write Access when system state == idle)

Addr: 0x1A06		**CURR2**		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*curr2*	0x0	RW	LED current for channel 2. Used for internal sensing. 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*
15:8	*curr2_target*	0x0	RW	Target LED current for channel 2 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*

8.1.5 CURR3 register (Address 0x1A08)

Table 16: CURR3 register

Addr: 0x1A08		CURR3		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*curr3*	0x0	RW	LED current for channel 3. Used for internal sensing. 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*
15:8	*curr3_target*	0x0	RW	Target LED current for channel 3 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*

8.1.6 CURR4 register (Address 0x1A0A)

Table 17: CURR4 register (Write Access when system state == idle)

Addr: 0x1A0A		CURR4		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*curr4*	0x0	RW	LED current for channel 4. Used for internal sensing. 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*
15:8	*curr4_target*	0x0	RW	Target LED current for channel 4 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*

8.1.7 CURR5 register (Address 0x1A0C)

Table 18: CURR5 register (Write Access when system state == idle)

Addr: 0x1A0C		CURR5		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*curr5*	0x0	RW	LED current for channel 5. Used for internal sensing. 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*
15:8	*curr5_target*	0x0	RW	Target LED current for channel 5 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*

8.1.8 CURR6 register (Address 0x1A0E)

Table 19: CURR6 register (Write Access when system state == idle)

Addr: 0x1A0E		CURR6		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*curr6*	0x0	RW	LED current for channel 6. Used for internal sensing. 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*
15:8	*curr6_target*	0x0	RW	Target LED current for channel 6 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*

8.1.9 CURR7 register (Address 0x1A10)

Table 20: CURR7 register (Write Access when system state == idle)

Addr: 0x1A10		CURR7		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*curr7*	0x0	RW	LED current for channel 7. Used for internal sensing. 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*
15:8	*curr7_target*	0x0	RW	Target LED current for channel 7 00h: 0mA 01h: 250µA 02h: 500µA 28h: 10mA 50h: 20mA 78h: 30mA FFh: 64mA **Note:** *Both fields currx and currx_target shall be programed to the same value.*

8.1.10 CURR_LIM0 register (Address 0x1A12)

Table 21: CURR_LIM0 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A12		CURR_LIM0		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*curr_lim0*	0x0	RW	LED current limits for channel 0 Upper limit defined in bits [15:8] Lower limit defined in bits [7:0]

8.1.11 CURR_LIM1 register (Address 0x1A14)

Table 22: CURR_LIM1 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A14		CURR_LIM1		
Bit	Bit field	Default	Access	Bit description
15:0	*curr_lim1*	0x0	RW	LED current limits for channel 1 Upper limit defined in bits [15:8] Lower limit defined in bits [7:0]

8.1.12 CURR_LIM2 register (Address 0x1A16)

Table 23: CURR_LIM2 register

Addr: 0x1A16		CURR_LIM2		
Bit	Bit field	Default	Access	Bit description
15:0	*curr_lim2*	0x0	RW	LED current limits for channel 2 Upper limit defined in bits [15:8] Lower limit defined in bits [7:0]

8.1.13 CURR_LIM3 register (Address 0x1A18)

Table 24: CURR_LIM3 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A18		CURR_LIM3		
Bit	Bit field	Default	Access	Bit description
15:0	*curr_lim3*	0x0	RW	LED current limits for channel 3 Upper limit defined in bits [15:8] Lower limit defined in bits [7:0]

8.1.14 CURR_LIM4 register (Address 0x1A1A)

Table 25: CURR_LIM4 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A1A		CURR_LIM4		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*curr_lim4*	0x0	RW	LED current limits for channel 4 Upper limit defined in bits [15:8] Lower limit defined in bits [7:0]

8.1.15 CURR_LIM5 register (Address 0x1A1C)

Table 26: CURR_LIM5 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A1C		CURR_LIM5		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*curr_lim5*	0x0	RW	LED current limits for channel 5 Upper limit defined in bits [15:8] Lower limit defined in bits [7:0]

8.1.16 CURR_LIM6 register (Address 0x1A1E)

Table 27: CURR_LIM6 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A1E		CURR_LIM6		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*curr_lim6*	0x0	RW	LED current limits for channel 6 Upper limit defined in bits [15:8] Lower limit defined in bits [7:0]

8.1.17 CURR_LIM7 register (Address 0x1A20)

Table 28: CURR_LIM7 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A20		CURR_LIM7		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*curr_lim7*	0x0	RW	LED current limits for channel 7 Upper limit defined in bits [15:8] Lower limit defined in bits [7:0]

8.1.18 CH_GROUP register (Address 0x1A22)

Table 29: CH_GROUP register (Write Access when system state == idle)

Addr: 0x1A22		CH_GROUP			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
6:0	*Chan_group*	0x0	RW	Channel group code for channels 0 to 6. The register has to be filled from bit 0 to 6: Set a '1' to define the start of a channel group. Set a '0' to define that the corresponding channel belongs to the same group. A group is only built when at least one channel in the group is enabled.	
				0	8 groups with each 1 channel inside
				Others	Bit 0 will be internally overwritten to 1 (channel 0 builds the first group)
				Note that channel 7 cannot be in an own group	

8.1.19 CH_DLY register (Address 0x1A24)

Table 30: CH_DLY register (Write Access when system state == idle)

Addr: 0x1A24		CH_DLY		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
9:0	*td_trigdly*	0x0	RW	Trigger delay [µs] 000h: 45µs 064h: 100µs 3FFh: 1024µs **Note:** Values < 45 are internally limited to a minimum of 45 [µs]
13:10	*td_stagger*	0x0	RW	Channel-to-channel delay for all channels in trigger group 0 Step size 1 µs

8.1.20 CH_ENABLE register (Address 0x1A26)

Table 31: CH_ENABLE register (Write Access when system state == idle)

Addr: 0x1A26		CH_ENABLE		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*Chan_enable*	0x0	RW	Channel enable vector, bit n enables channel [n]

8.1.21 LED_CONFIG register (Address 0x1A28)

Table 32: LED_CONFIG register (Write Access when system state == idle)

Addr: 0x1A28		LED_CONFIG		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*Led_config*	0x0	RW	**LED configuration per channel** 0 — 1-LED 1 — 2-LEDs
10	*led_fb_ov_mask*	0x0	RW	Masks overvoltage detection for all channels configured as 1-LED channel

8.1.22 CH_SLEW30 register (Address 0x1A2C)

Table 33: CH_SLEW30 register (Write Access when system state == idle)

Addr: 0x1A2C		CH_SLEW30			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
15:0	*Slew30*	0x0	RW	Number of slew steps time and slew time, controlled by 4 bits per channel glob_slew_enable needs to be 1 to turn on channel slew / bit[3:0]..ch0, bit[7:4]..ch1, bit[11:8]..ch2, bit[15:12]..ch3	
				0	Slew time = 0µs, 1 step
				1	Slew time = 0.3µs, 4 steps (100ns step time)
				2	Slew time = 0.7µs, 8 steps (100ns step time)
				3	Slew time = 0.6µs, 4 steps (200ns step time)
				4	Slew time = 1.5µs, 16 steps (100ns step time)
				5	Slew time = 1.4µs, 8 steps (200ns step time)
				6	Slew time = 1.2µs, 4 steps (400ns step time)
				7	Slew time = 3.0µs, 16 steps (200ns step time)
				8	Slew time = 2.8µs, 8 steps (400ns step time)
				9	Slew time = 2.4µs, 4 steps (800ns step time)

8.1.23 CH_SLEW74 register (Address 0x1A2E)

Table 34: CH_SLEW74 register (Write Access when system state == idle)

Addr: 0x1A2E	CH_SLEW74				
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
15:0	*Slew74*	0x0	RW	Number of slew steps time and slew time, controlled by 4 bits per channel glob_slew_enable needs to be 1 to turn on channel slew bit[3:0]..ch0, bit[7:4]..ch1, bit[11:8]..ch2, bit[15:12]..ch3	
				0	Slew time = 0µs, 1 step
				1	Slew time = 0.3µs, 4 steps (100ns step time)
				2	Slew time = 0.7µs, 8 steps (100ns step time)
				3	Slew time = 0.6µs, 4 steps (200ns step time)
				4	Slew time = 1.5µs, 16 steps (100ns step time)
				5	Slew time = 1.4µs, 8 steps (200ns step time)
				6	Slew time = 1.2µs, 4 steps (400ns step time)
				7	Slew time = 3.0µs, 16 steps (200ns step time)
				8	Slew time = 2.8µs, 8 steps (400ns step time)
				9	Slew time = 2.4µs, 4 steps (800ns step time)

8.1.24 CH_CONTROL register (Address 0x1B48)

Table 35: CH_CONTROL register (Write Access when system state == idle)

Addr: 0x1B48		CH_CONTROL			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
2	*glob_slew_enable*	0x0	RW	**Global channel slew control**	
				0	Channel slew off
				1	Channel slew on

8.1.25 HSCS_SEL register (Address 0x1A30)

Table 36: HSCS_SEL register (Write Access when otp_cust_lock ==0)

Addr: 0x1A30		HSCS_SEL		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
3:0	*hs_currs_nr_chan*	0x0	RW	Range setting for High-side current sensing **0 Do not use** 1 Sensing range 1 <100mA 2 Sensing range 2 100mA to 300mA 3 Sensing range 3 300mA to 400mA 4 Sensing range 4 400mA to 600mA 5 Sensing range 5 500mA to 700mA 6 Sensing range 6 500mA to 900mA 7 Sensing range 7 600mA to 1000mA 8 Sensing range 8 700mA to 1000mA 9 Sensing range 9 800mA to 1000mA 10 Sensing range 10 900mA to 1000mA
5:4	*Hs_currs_lp_pullup*	0x0	RW	Select LP pull-up current to compensate for parasitic capacitance in transition to illum. 0 Default LP pull-up current (~150µA) 1 LP pull-up current = 2x of default value 2 LP pull-up current = 3x of default value 3 LP pull-up current = 4x of default value
15:8	*hs_set_iref*	0x0	RW	Reference current in 1µA Steps (do not use numbers below 12µA) 0 — 0 — No reference Current --> This setting always Trigger Fault when high-side current sensing enabled **1 to 11 — 1µA to 11µA — Do not use** 12 — 12µA — For sensing ~50mA 50 — 50µA — For sensing 200mA select this setting 100 — 100µA — For sensing 400mA select this setting 195 — 195µA — For sensing 780mA select this setting 250 — 250µA — For sensing 1A select this setting

8.1.26 PWM_CTR register (Address 0x1A32)

Table 37: PWM_CTR register (Write Access when otp_cust_lock ==0)

Addr: 0x1A32		PWM_CTR		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
0	*pwm_illum_enable*	0x0	RW	LED illumination duration is controlled by STROBE_PWM1 input used as PWM source. **Note:** If enabled td_illum shows sampled illumination duration safety trigger signal test is forced to be disabled if this bit is high safety illumination max test is forced to be disabled if STROBE input is high for more than 32768 µs if this bit is high
7:4	*pwm_grp_split*	0x0	RW	Enable ID2_PWM2 as the secondary input and select for PWM into two groups. **Note:** If set > 0, indicates channel number starting from which illumination is controlled by ID2 input i.e., if set to 4, channels 0-3 illumination duration is controlled by STROBE input, channels 4-7 is controlled by ID2/STROBE_AUX input if set to 0, all channels illumination duration is controlled by STROBE input.
9:8	*pwm_trig*	0x0	RW	Trigger control for the mode with ID2 as auxiliary strobe input defines how illumination sequence for both main(STROBE) and auxiliary(ID2) channels group is triggered. 0 – Default, STROBE or ID2, illumination is triggered by the first coming edge either ID2 or STROBE signal 1 – STROBE and ID2, illumination is triggered in the moment both STROBE and ID2 become high 2 – STROBE only, illumination for both groups is triggered only by the STROBE signal rising edge 3 – ID2 only, illumination for both groups is triggered only by the ID2 signal rising edge

8.1.27 TD_TRATE_MAX register (Address 0x1A34)

Table 38: TD_TRATE_MAX register (Write Access when otp_cust_lock ==0)

Addr: 0x1A34		TD_TRATE_MAX		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
13:0	*td_trigrate_max*	0x0	RW	td_trigrate_max limit for safety check, with a resolution of 16µs (allows 1Hz resolution in the range between 5-250Hz) Calculation: td_trigrate_max = floor((TRATE_ideal[µs] - 17.0655) / 16.5358) TRATE_safefail[µs] = TD_RATE_MAX * 15.49787 - 16.0863. (all trigger delays lower than this limit will generate a FAULT) TRATE_nofail[µs] = TD_RATE_MAX * 16.53576 + 17.0447. (all trigger delays longer than this limit will never generate a FAULT) 250 4.000ms period (250Hz) 251 4.016ms period (249Hz) .. ... 12093 200ms period (5Hz)

8.1.28 TD_ILLUM_MAX register (Address 0x1A36)

Table 39: TD_ILLUM_MAX register (Write Access when otp_cust_lock ==0)

Addr: 0x1A36		TD_ILLUM_MAX		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*td_illum_max*	0x0	RW	td_illum_max limit for safety check, resolution: 1µs limit depends on the values of register td_illum, td_stagger, chan_enable and slew settings and is calculated as td_illum_max = td_illum + (number_active_groups - 1) * td_stagger + slew_time_last_channel DEC 100 -> 0x0064 -> 100µs DEC 1000 -> 0x03E8 -> 1ms DEC 5000 -> 0x1388 -> 5ms DEC 15000 -> 0x3A98 -> 15ms (maximum value) >=DEC 15001 (do not use) **Note:** In PWM mode ON time is constrained to be maximum 15ms. Therefore, the value in the TD_ILLUM_MAX register shall be less the 15ms in this mode.

8.1.29 IRQ_ENABLE0 register (Address 0x1A38)

Table 40: IRQ_ENABLE0 register (Write Access when diagnostic mode ==1)

Addr: 0x1A38 **IRQ_ENABLE0**

Bit	Bit field	Default	Access	Bit description		
15:0	*Irq_enable*	0x0	RW	**Bit n: Interrupt is enabled when bit is set, otherwise disabled interrupt sources:**		
				0	fault	System fault (OR-function of all critical faults)
				1	fv_tc_done	temp. compensation done
				2	vload_adj_request	vload adjust request
				3	asic_test_done	run_self test complete
				4	boot_complete	Boot-up complete (before entering IDLE after startup)
				5	task_done	Task done in config mode
				6	periodic_test_done	Periodic test done
				7	illum_start	Illumination start
				8	illum_end	Illumination end trigger
				9	over_temp	Temperature > 125deg.C
				10	idrive_overvoltage	Overvoltage on any active channel
				11	idrive_undervoltage	Undervoltage on any active channel
				12	trigger_rate_error	Trigger rate error ("min_timer") - This safety related interrupt is automatically enabled during its BIST
				13	otp_ecc_error	asserted by otp during OTP read
				14	idrive_ramp_error	Error when a channel ramps down before ramp-up has completed
				15	illum_duration_error	Illumination on-time overrun error - This safety related interrupt is automatically enabled during its BIST

8.1.30 IRQ_ENABLE1 register (Address 0x1A3A)

Table 41: IRQ_ENABLE1 register (Write Access when diagnostic mode ==1)

Addr: 0x1A3A **IRQ_ENABLE1**

Bit	Bit field	Default	Access	Bit description		
15:0	*irq_enable[31:16]*	0x0	RW	**Bit n: Interrupt is enabled when bit is set, otherwise disabled interrupt sources:**		
				0	osc_error	Oscillator period check error - This safety related interrupt is automatically enabled during its BIST
				1	watchdog_timeout	Watchdog timeout
				2	rload_test_error	Rload test fail
				3	hs_overcurrent	HS switch overcurrent BIST error
				4	curr_lim_hi_overrun	Overcurrent error on any channel
				5	curr_lim_lo_underrun	Undercurrent error on any channel
				6	supply_overvoltage	Overvoltage error on VP18 or Vload
				7	supply_undervoltage	Undervoltage error on VP18 or Vload
				8	lp_short_open_error	LP short or open error
				9	ln_short_open_error	LN short or open error
				10	idrive_feedback_error	Idrive vs. analog current comparison
				11	otp_test_error	OTP read check error
				12	ram_bist_error	RAM BIST error - Enabled by default
				13	rom_bist_error	ROM BIST error - Enabled by default
				14	Not used	
				15	Not used	

8.1.31 IRQ_ENABLE2 register (Address 0x1A3C)

Table 42: IRQ_ENABLE2 register (Write Access when diagnostic mode ==1)

<table>
<tr><th colspan="2">Addr: 0x1A3C</th><th colspan="5">IRQ_ENABLE2</th></tr>
<tr><th>Bit</th><th>Bit field</th><th>Default</th><th>Access</th><th colspan="3">Bit description</th></tr>
<tr><td rowspan="8">6:0</td><td rowspan="8">irq_enable[38:32]</td><td rowspan="8">0x0</td><td rowspan="8">RW</td><td colspan="3">Bit n: Interrupt is enabled when bit is set, otherwise disabled</td></tr>
<tr><td>0</td><td>vload_monitor_error</td><td>vload monitor BIST fail</td></tr>
<tr><td>1</td><td>vp18_monitor_error</td><td>vp18 monitor BIST fail</td></tr>
<tr><td>2</td><td>temp_detect_error</td><td>Temperature detector BIST fail</td></tr>
<tr><td>3</td><td>adc_bist_error</td><td>ADC BIST fail</td></tr>
<tr><td>4</td><td>ls_overcurrent</td><td>Driver gate low -> low side overcurrent</td></tr>
<tr><td>5</td><td>driver_gate_short</td><td>Driver gate short</td></tr>
<tr><td>6</td><td>ldo_overcurrent</td><td>LDO overcurrent</td></tr>
</table>

8.1.32 CONFIG_KEY_COMP0 register (Address 0x1A42)

Table 43: CONFIG_KEY_COMP0 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A42		CONFIG_KEY_COMP0		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*Key_compare[15:0]*	0xc7a6	RW	LSB of key which is used for comparing

8.1.33 CONFIG_KEY_COMP1 register (Address 0x1A44)

Table 44: CONFIG_KEY_COMP1 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A44		CONFIG_KEY_COMP1		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*Key_compare[31:16]*	0x13bf	RW	LSB of key which is used for comparing

8.1.34 CUSTLOCK register (Address 0x1A46)

Table 45: CUSTLOCK register (Write Access when otp_cust_lock ==0)

Addr: 0x1A46		CUSTLOCK			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
0	*otp_cust_lock*	0x0	RW	**Lock bit for customer section in the OTP, lock bit cannot be cleared when set**	
				0	OTP section is not programmed
				1	OTP section is programmed and write access is locked
				Note: Lock bit is sticky and cannot be cleared when once set	

8.1.35 COMP_LVL_LOW register (Address 0x1A48)

Table 46: COMP_LVL_LOW register (Write Access when otp_cust_lock ==0)

Addr: 0x1A48		COMP_LVL_LOW			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
1:0	*sel_vds_window_low*	0x1	RW	**DCDC - Feedback low voltage detection comparator**	
				0	200mV Detection Level
				1	250mV Detection Level (Default)
				2	300mV Detection Level
				3	400mV Detection Level

8.1.36 COMP_LVL_HIGH register (Address 0x1A4A)

Table 47: COMP_LVL_HIGH register (Write Access when otp_cust_lock ==0)

Addr: 0x1A4A		COMP_LVL_HIGH			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
1:0	*sel_vds_window_high*	0x2	RW	**DCDC - Feedback high voltage detection comparator**	
				0	800mV Detection Level
				1	400mV Detection Level
				2	500mV Detection Level (Default)
				3	650mV Detection Level

8.1.37 COMP_LVL_SHORT register (Address 0x1A4C)

Table 48: COMP_LVL_SHORT register (Write Access when otp_cust_lock ==0)

Addr: 0x1A4C		COMP_LVL_SHORT			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
1:0	*sel_vshort*	0x0	RW	**Shortled detection voltage**	
				0	600mV detection level (Default)
				1	400mV detection level
				2	1.0V detection level
				3	0.8V detection level

8.1.38 COMP_LVL_OPEN register (Address 0x1A4E)

Table 49: COMP_LVL_OPEN register (Write Access when otp_cust_lock ==0)

Addr: 0x1A4E		COMP_LVL_OPEN			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
0	*sel_vopen*	0x0	RW	**OpenLed detection voltage**	
				0	50mV detection level (default)
				1	100mV detection level

8.1.39 CTRL_PADS1 register (Address 0x1A58)

Table 50: CTRL_PADS1 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A58		CTRL_PADS1		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
0	*Id0_rpu_en*	0x0	RW	1.. internal pullup enabled for ID0
1	*Id1_rpu_en*	0x0	RW	1.. internal pullup enabled for ID1
2	*strobe2_rpu_en*	0x0	RW	1.. internal pullup enabled for Strobe 2
3	*test_rpu_en*	0x0	RW	1.. internal pullup enabled for Test
4	*strobe1_rpu_en*	0x0	RW	1.. internal pullup enabled for Strobe 1
5	*irqn_rpu_en*	0x1	RW	1.. internal pullup enabled for IRQN
8	*Id0_rpd_en*	0x1	RW	1.. internal pulldown enabled for ID0
9	*Id1_rpd_en*	0x1	RW	1.. internal pulldown enabled for ID1
10	*strobe2_rpd_en*	0x1	RW	1.. internal pulldown enabled for Strobe 2
11	*test_rpd_en*	0x1	RW	1.. internal pulldown enabled for Test
12	*strobe1_rpd_en*	0x1	RW	1.. internal pulldown enabled for Strobe 1
13	*irqn_rpd_en*	0x0	RW	1.. internal pulldown enabled for IRQN
14	*scl_drv_i2c_1v2_en*	0x0	RW	1.. increase drive strength of SCL pin in case of VBUS = 1.2V
15	*sda_drv_i2c_1v2_en*	0x0	RW	1.. increase drive strength of SDA pin in case of VBUS = 1.2V

(1) If both rpu and rpd are enabled, pulldown will be used. If both rpu and rpd are disabled, pad must not be left floating.

8.1.40 DEVICE_REV register (Address 0x1A5C)

Table 51: DEVICE_REV register (Write Access when otp_cust_lock ==0)

Addr: 0x1A5C		DEVICE_REV		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
11:0	*Device_rev*	0x0	RO	**Device Revision**

8.1.41 DEVICE_UID0 register (Address 0x1A5E)

Table 52: DEVICE_UID0 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A5E		DEVICE_UID0		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*device_uid0*	0x0	RO	**Unique Device ID**

8.1.42 DEVICE_UID1 register (Address 0x1A60)

Table 53: DEVICE_UID1 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A60		DEVICE_UID1		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*device_uid1*	0x0	RO	**Unique Device ID**

8.1.43 DEVICE_UID2 register (Address 0x1A62)

Table 54: DEVICE_UID2 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A62		DEVICE_UID2		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*device_uid2*	0x0	RO	**Unique Device ID**

8.1.44 CTRL_PADS0 register (Address 0x1A64)

Table 55: CTRL_PADS0 register (Write Access when otp_cust_lock ==0)

Addr: 0x1A64		CTRL_PADS0		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
1	*Strobe1_input_ena*	0x0	RW	Input enable for Strobe 1 pad 0…off 1…enabled
4	*Pad_opendrain*	0x1	RW	Open drain control for IRQ_N pad 0…push/pull 1…open drain
5	*Id0_input_ena*	0x1	RW	Input enable for ID0 pad 1…enabled
6	*Id1_input_ena*	0x1	RW	Input enable for ID1 pad 1…enabled
7	*Strobe2_input_ena*	0x1	RW	Input enable for Strobe2 pad 0…off 1…enabled
10	*Test_pin_status*	0x0	RO	Status of Test pin 0…pin is low 1…pin is high

8.1.45 STAT_VISOURCE register (Address 0x1A80)

Table 56: STAT_VISOURCE register (Write Access when otp_cust_lock ==0)

Addr: 0x1A80		STAT_VISOURCE		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
0	*Overtemp_60*	0x0	RO	Over temperature Warning 60 Degree C 1.. temperature >60C
1	*Overtemp_120*	0x0	RO	Over temperature Warning 120 Degree C 1.. temperature >120C
2	*Overtemp_140*	0x0	RO	Over temperature Warning 140 Degree C 1.. temperature >140C
3	*undertemp_m20*	0x0	RO	Under temperature Warning -20 Degree C 1.. temperature < -20C

8.1.46 STAT_SUPPLY register (Address 0x1A94)

Table 57: STAT_SUPPLY register (Write Access when otp_cust_lock ==0)

Addr: 0x1A94		STAT_SUPPLY		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
0	*VP18_OV*	0x0	RO	VP18 overvoltage information 1.. VP18 overvoltage condition
1	*VP18_UV*	0x0	RO	VP18 undervoltage information 1.. VP18 undervoltage condition
2	*VLED_OV*	0x0	RO	VLED overvoltage information 1.. VLED overvoltage condition
3	*VLED_UV*	0x0	RO	VLED undervoltage information 1.. VLED undervoltage condition
4	*reserved*	0x0	RO	
5	*reserved*	0x0	RO	
6	*reserved*	0x0	RO	

8.1.47 TASK_DISABLE0 register (Address 0x1B40)

Table 58: TASK_DISABLE0 register (Write Access when otp_cust_lock ==0)

Addr: 0x1B40		TASK_DISABLE0		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*task_disable0*	0x0	RW	Individual task low disable (only use in case that a task/Bist fails). CPU ignores RAM/ROM/RLOAD/VF BISTs & VP18 monitor when set.

8.1.48 TASK_DISABLE1 register (Address 0x1B42)

Table 59: TASK_DISABLE1 register (Write Access when otp_cust_lock ==0)

Addr: 0x1B42		**TASK_DISABLE1**		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*task_disable1*	0x0	RW	Individual task high disable (only use in case that a task/Bist fails). CPU ignores RAM/ROM/RLOAD/VF BISTs & VP18 monitor when set. Ensure all interrupts are handled before manual BIST is executed.

8.1.49 TASK_DISABLE2 register (Address 0x1B44)

Table 60: TASK_DISABLE2 register (Write Access when otp_cust_lock ==0)

Addr: 0x1B44		**TASK_DISABLE2**		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*task_disable2*	0x0	RW	Individual task ccc disable Task disable 3 maps to ccc task.

8.1.50 I3C_CONFIG register (Address 0x1B4A)

Table 61: I3C_CONFIG register (Write Access when otp_cust_lock ==0)

Addr: 0x1B4A		I3C_CONFIG			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
0	*i3c_device*	0x0	RW	**I3C/I²C default mode**	
				0	I²C mode
				1	I3C mode
1	*en_i3c_detect*	0x1	RW	**Automatic I3C bus detection enable**	
				0	Off
				1	On
2	*en_i3c_ibi*	0x0	RW	**Enable in-band interrupt feature**	
				0	Off
				1	On
7:6	*i3c_inst_id*	0x0	RW	I3C instance ID	
15:8	*i3c_dcr*	0x0	RW	I3C device characteristic register	

8.1.51 I3C_PART_ID register (Address 0x1B4C)

Table 62: I3C_PART_ID register (Write Access when otp_cust_lock ==0)

Addr: 0x1B4C		I3C_PART_ID		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*i3c_part_id*	0x0	RW	I3C part ID

8.1.52 IRQ_STATUS0 register (Address 0x1AA4)

Table 63: IRQ_STATUS0 register

Addr: 0x1AA4		IRQ_STATUS0		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*irq_status[15:0]*	0x0	PUSHPOP	0 fault 1 reserved 2 vload_adj_request 3 asic_test_done 4 boot_complete 5 task_done 6 periodic_test_done 7 illum_start 8 illum_end 9 over_or_under_temp 10 idrive_overvoltage 11 idrive_undervoltage 12 trigger_rate_error 13 otp_ecc_error 14 idrive_ramp_error 15 illum_duration_error

8.1.53 IRQ_STATUS1 register (Address 0x1AA6)

Table 64: IRQ_STATUS1 register

Addr: 0x1AA6		IRQ_STATUS1		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*irq_status[31:16]*	0x0	PUSHPOP	0 osc_error 1 watchdog_timeout 2 rload_test_error 3 hs_overcurrent 4 curr_lim_hi_overrun 5 curr_lim_lo_underrun 6 supply_overvoltage 7 supply_undervoltage 8 lp_short_open_error 9 ln_short_open_error 10 idrive_feedback_error 11 otp_test_error 12 ram_bist_error 13 rom_bist_error

8.1.54 IRQ_STATUS2 register (Address 0x1AA8)

Table 65: IRQ_STATUS2 register

Addr: 0x1AA8		IRQ_STATUS2		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
6:0	*irq_status[38:32]*	0x0	PUSHPOP	0 vload_monitor_error 1 vp18_monitor_error 2 temp_detect_error 3 adc_bist_error 4 ls_overcurrent 5 driver_gate_short 6 ldo_overcurrent

8.1.55 IRQ_HISTORY0 register (Address 0x1AAA)

Table 66: IRQ_HISTORY0 register (Access Read Only)

Addr: 0x1AAA		IRQ_HISTORY0		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*irq_history[15:0]*	0x0	RW_SM	Copy of the interrupt status register0 before Interrupt status0 is cleared 0 fault 1 reserved 2 vload_adj_request 3 asic_test_done 4 boot_complete 5 task_done 6 periodic_test_done 7 illum_start 8 illum_end 9 over_or_under_temp 10 idrive_overvoltage 11 idrive_undervoltage 12 trigger_rate_error 13 otp_ecc_error 14 idrive_ramp_error 15 illum_duration_error

8.1.56 IRQ_HISTORY1 register (Address 0x1AAC)

Table 67: IRQ_HISTORY1 register (Access Read Only)

Addr: 0x1AAC		IRQ_HISTORY1		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*irq_history[31:16]*	0x0	RW_SM	Copy of the interrupt status register1 before Interrupt status1 is cleared 0 osc_error 1 watchdog_timeout 2 rload_test_error 3 hs_overcurrent 4 curr_lim_hi_overrun 5 curr_lim_lo_underrun 6 supply_overvoltage 7 supply_undervoltage 8 lp_short_open_error 9 ln_short_open_error 10 idrive_feedback_error 11 otp_test_error 12 ram_bist_error 13 rom_bist_error

8.1.57 IRQ_HISTORY2 register (Address 0x1AAE)

Table 68: IRQ_HISTORY2 register (Access Read Only)

Addr: 0x1AAE		IRQ_HISTORY2		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
6:0	*irq_history[38:32]*	0x0	RW_SM	Copy of the interrupt status register2 before Interrupt status2 is cleared 0 vload_monitor_error 1 vp18_monitor_error 2 temp_detect_error 3 adc_bist_error 4 ls_overcurrent 5 driver_gate_short 6 ldo_overcurrent

8.1.58 IRQ_MASK0 register (Address 0x1AB0)

Table 69: IRQ_MASK0 register (Access Read Only)

Addr: 0x1AB0		IRQ_MASK0			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
15:0	*irq_mask[15:0]*	0x0	RW	**Bit n:**	
				0	Interrupt asserts IRQ_N (and I3C-IBI when enabled)
				1	Interrupt bit is inhibited from asserting IRQ_N and I3C-IBI

8.1.59 IRQ_MASK1 register (Address 0x1AB2)

Table 70: IRQ_MASK1 register (Write Access always)

Addr: 0x1AB2		IRQ_MASK1			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
15:0	*irq_mask[31:16]*	0x0	RW	**Bit n:**	
				0	Interrupt asserts IRQ_N (and I3C-IBI when enabled)
				1	Interrupt bit is inhibited from asserting IRQ_N and I3C-IBI

8.1.60 IRQ_MASK2 register (Address 0x1AB4)

Table 71: IRQ_MASK2 register (Write Access always)

Addr: 0x1AB4		IRQ_MASK2			
Bit	**Bit field**	**Default**	**Access**	**Bit description**	
6:0	*irq_mask[38:32]*	0x0	RW	**Bit n:**	
				0	Interrupt asserts IRQ_N (and I3C-IBI when enabled)
				1	Interrupt bit is inhibited from asserting IRQ_N and I3C-IBI

8.1.61 SYSTEM STATE register (Address 0x1AC4)

Table 72: SYSTEM STATE register (Read Only)

Addr: 0x1AC4	SYSTEM STATE					
Bit	**Bit field**	**Default**	**Access**	**Bit description**		
2:0	*system_state*	0x0	RO	**system_state**		
				0	Startup	CPU controlled state
				1	Idle	CPU controlled state
				2	Periodic	CPU controlled state
				3	Bist/rload	CPU controlled state
				4	Sleep	CPU controlled state
				5	Triggered	HW controlled state
				6	Illum	HW controlled state
				7	Fault	HW controlled state
3	*bist_busy*	0x0	RW	**Bist status (set by CPU)**		
				0		Idle
				1		Active
4	*bist_failed*	0x0	RW	**Bist status (set by CPU)**		
				0		Pass
				1		Fail
5	*configuration_mode*	0x0	RO	System is in configuration mode, entered by I3C CCC or writing I2C_COMMAND_CODE register		
8	*vfbist_on*	0x0	RW	Set by CPU during VF Bist (signal is used for VF current selection)		
9	*otp_bit_corrected*	0x0	RO	Set when at least one OTP bit was error corrected during OTP readout at boot		

8.1.62 CONFIG_KEY0 register (Address 0x1AC6)

Table 73: CONFIG_KEY0 register (Read only)

Addr: 0x1AC6		**CONFIG_KEY0**		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*Key[15:0]*	0x0	RW	Lower portion of the key modifiable for entering config mode - execute ChangeMode CCC after storing the key here to enter or exit CONFIG_MODE

8.1.63 CONFIG_KEY1 register (Address 0x1AC8)

Table 74: CONFIG_KEY1 register (Read only)

Addr: 0x1AC8		**CONFIG_KEY1**		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
15:0	*Key[31:16]*	0x0	RW	Upper portion of the key modifiable for entering config mode - execute ChangeMode CCC after storing the key here to enter or exit CONFIG_MODE

8.1.64 I2C_COMMAND_CODE register (Address 0x1ACA)

Table 75: I2C_COMMAND_CODE register (Write access always)

Addr: 0x1ACA		**I2C_COMMAND_CODE**		
Bit	**Bit field**	**Default**	**Access**	**Bit description**
7:0	*command_code*	0x0	PUSH	I²C command code register, writing I3C vendor command codes to this register when in I²C mode will trigger the respective command

9 Application information

In the following application schematics, the high-power infrared emitter SFH 4043 is considered. The LED is optimized for eye, face and hand tracking applications with a peak wavelength of 940nm. Figure 32 shows a typical application of 1xSFH 4043 per channel and Figure 33 is using 2xSFH 4043 per current sink.

9.1 Schematic

Figure 36: Recommended circuit 1 SFH 4043 IR LED application

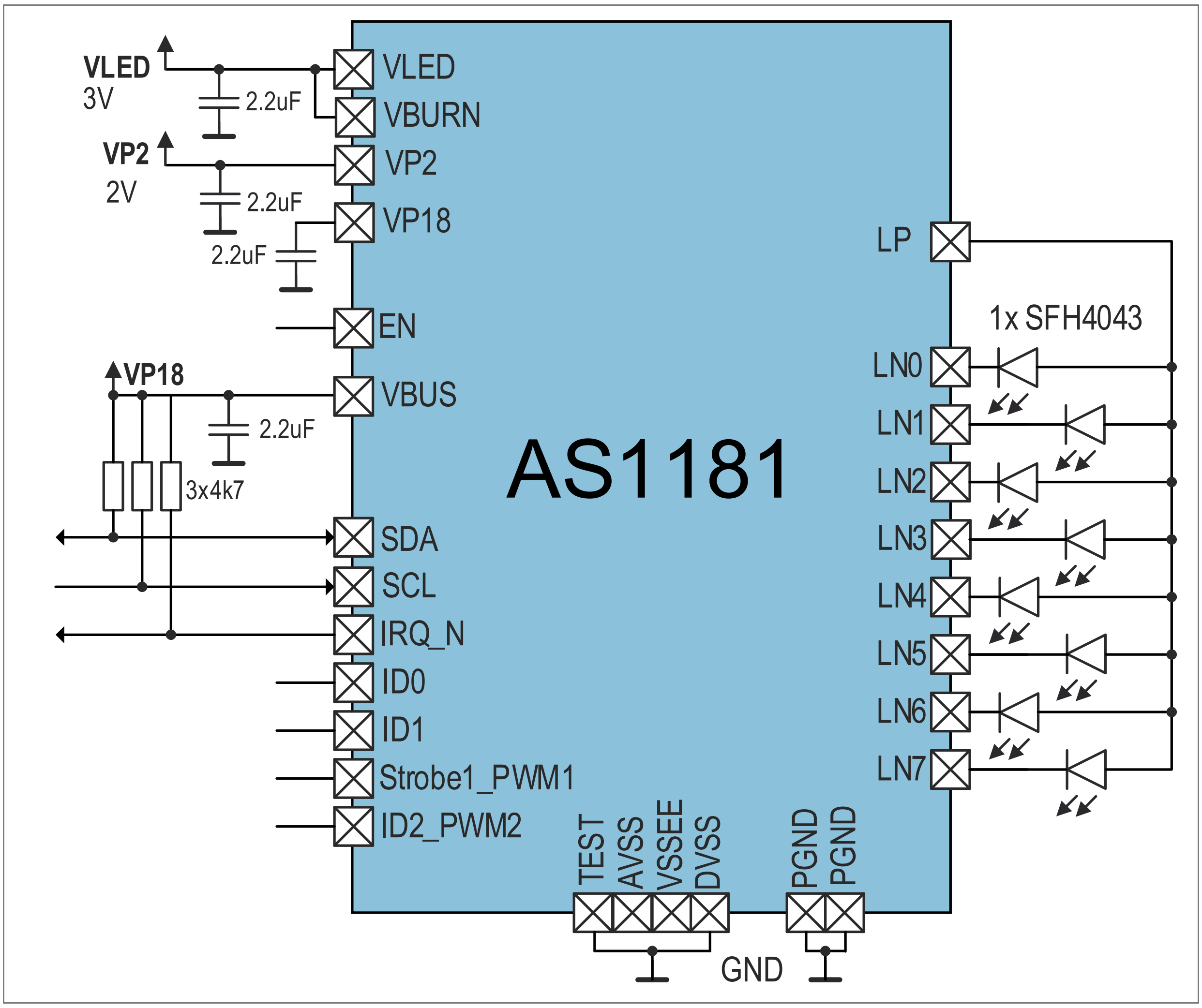
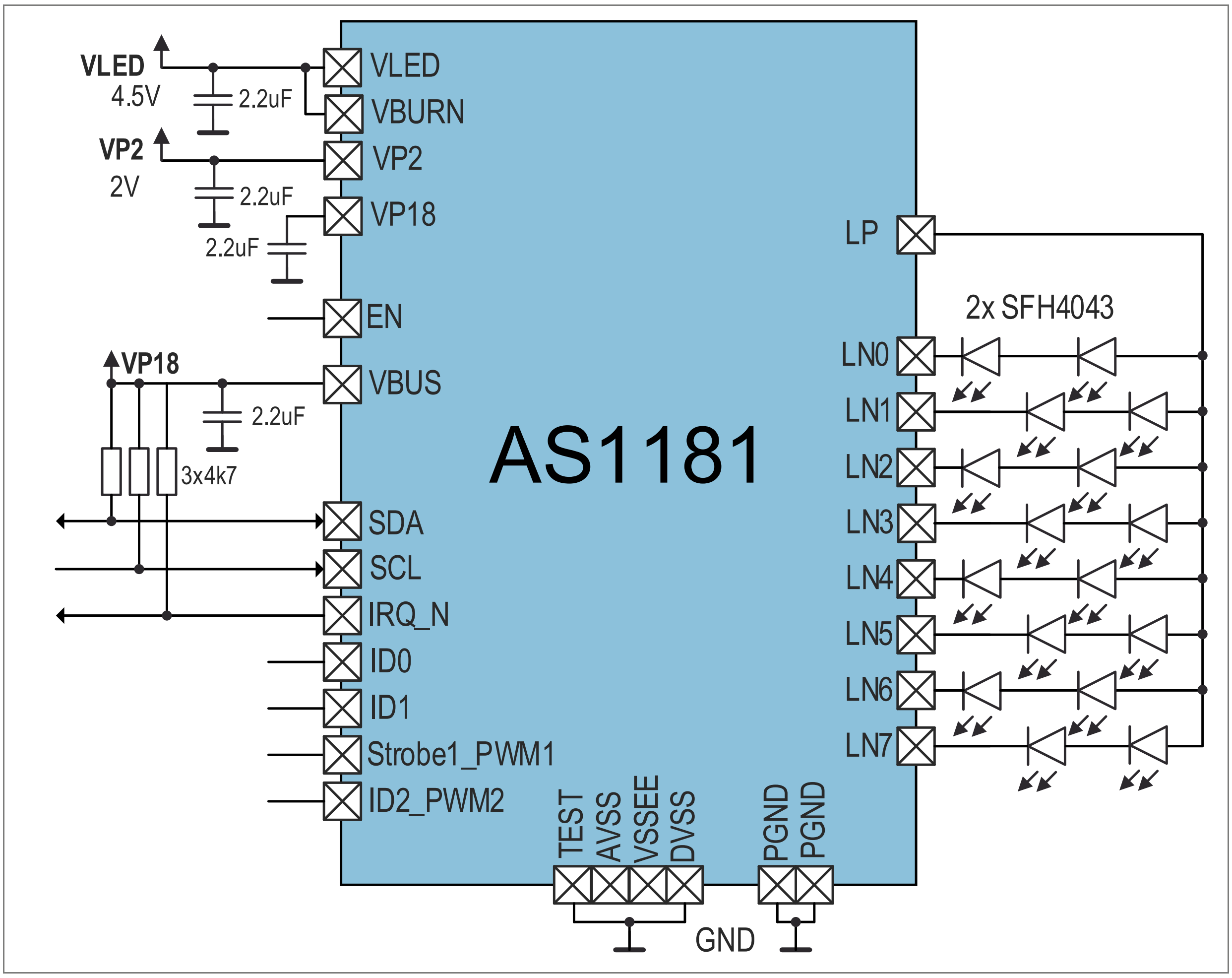
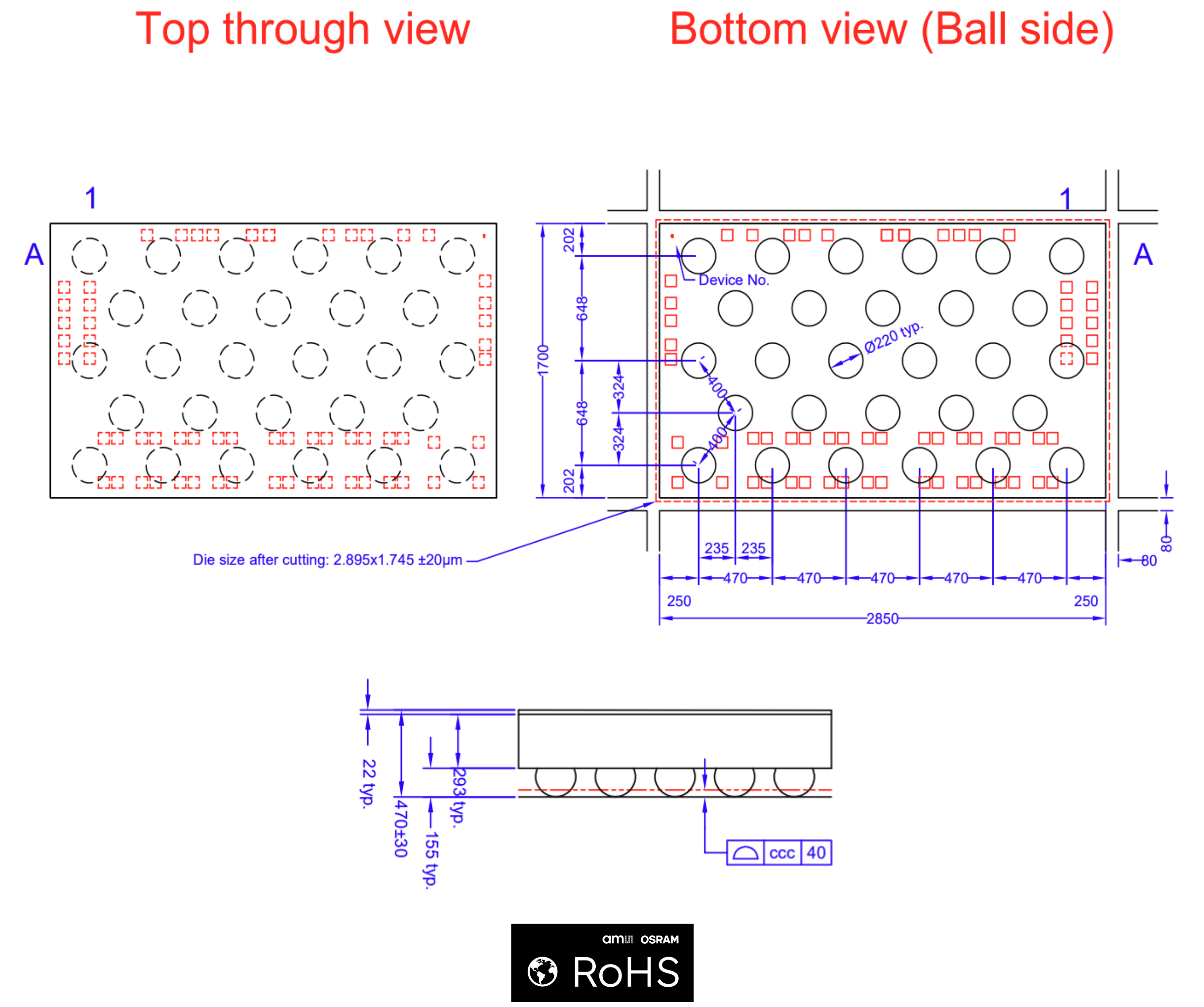


Figure 37: Recommended circuit 2 SFH 4043 IR LED application



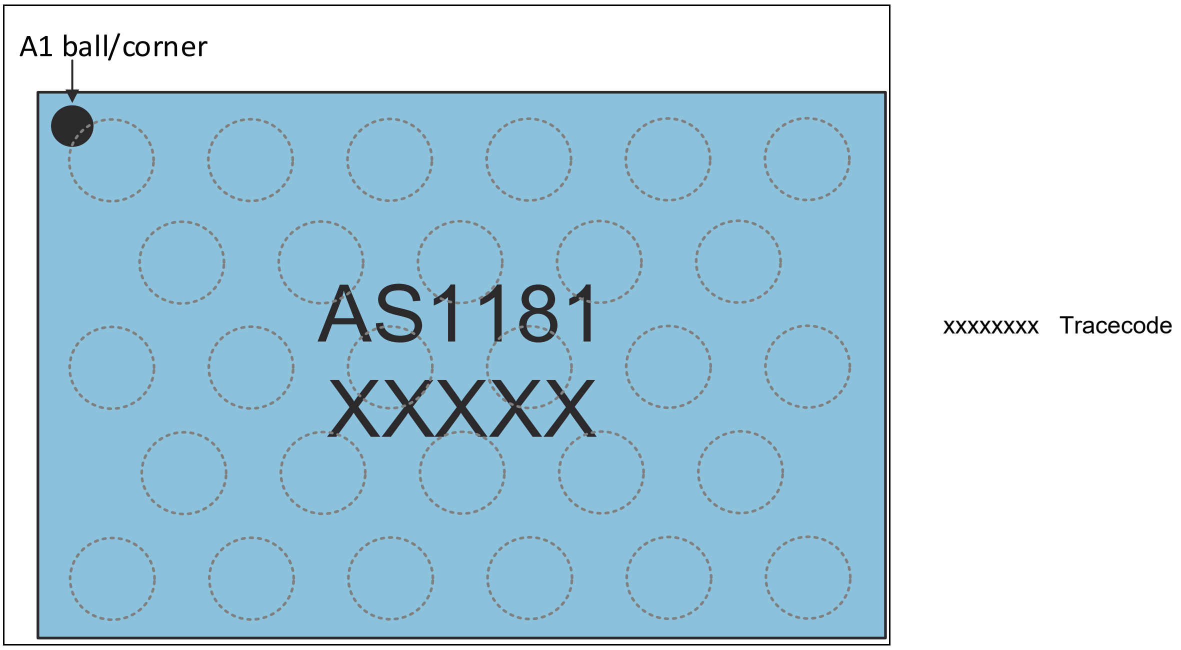
10 Package drawings & markings

Figure 38: AS1181 WLCSP28 package outline drawing



(1) All dimensions are in micrometers [µm]. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.

Figure 39: AS1181 package marking/code



11 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Changes from previous released version to current revision v1-00	Page
Initial production version	
Updated note under package drawings chapter 10	79

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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Headquarters

ams-OSRAM AG

Tobelbader Strasse 30

8141 Premstaetten

Austria, Europe

Tel: +43 (0) 3136 500 0

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